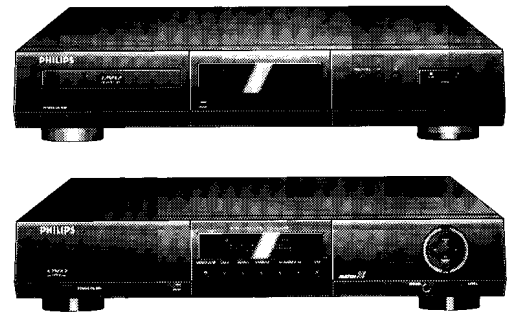


Service  
Service  
Service

# Service Manual

## INTRODUCTION

Philips DVD-Video Player introduction 1998

The ultimate video playback source for your Home Cinema. This sophisticated player delivers stunning digital video pictures, with digital multichannel sound, from revolutionary long-playing DVD-Video discs. As part of the new worldwide DVD standard,

The DVD730 and DVD 930 matchline also plays your existing Video CDs and audio CDs. And it features the simplest possible operation with easy-to-understand on-screen displays and menus, plus many brand-new convenience features.

- Plays new DVD-Video discs, plus Video CDs and Audio CDs
- Movies the way they were meant to be - on both wide-screen and regular TV screens
- Advanced DVD-MPEG 2 Video technology includes dual-lens optical pickup, 10-bit video DAC, RGB component video output, cascade 4-stage FIR audio filter, Bitstream continuous calibration D/A converter.
- Digital audio output for MPEG2 Digital Multichannel, Dolby Digital<sup>®</sup> (AC-3) and PCM
- Multistandard (PAL/NTSC) video with studio-quality resolution
- Analogue audio output for Dolby Pro Logic<sup>®</sup> and stereo
- Supports multi-angle camera shots, storyline variations, up to 8 spoken languages, and up to 32 subtitle languages
- Advanced on-screen menus with choice of languages
- Full-feature remote control
- Perfect still pictures and variable speed control
- Unique Philips Parental Control

## SERVICING

The repair of the DVD player is divided in 1<sup>st</sup> and 2<sup>nd</sup> line .  
1<sup>st</sup> line service for all workshops repair to component level : Power supply ; AV pcb ; Keyboard and display pcb and cabinet .**No repair of Basic engine and Digital pcb**  
2<sup>nd</sup> line service for central workshop from PCS : DVD mechanism (Basic Engine) and Digital main pcb.

Diagnostics: the players are equipped with embedded dedicated service software for dealer and 1<sup>st</sup> line service

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10. Power supply board
11. Headphone & Display board
12. A/V-MUX board

COMPACT  
disc  
DIGITAL AUDIOCOMPACT  
disc  
DIGITAL VIDEODVD  
VIDEOCLASS 1  
LASER PRODUCT

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## TECHNICAL SPECIFICATIONS

### General

Mains voltage :	100-240V +10%/-15%
Mains frequency :	50-60 Hz
DC output :	+5V $\pm$ 10% ;50mA max
Power consumption mains :	23W (typical)
Power consumption standby :	$\leq$ 5W

### Audio performance

#### Line output

- Output voltage : 2V +/- 1.5dB
- Channel unbalance (1kHz) : < 0.85dB
- Crosstalk :
  - 1kHz : > 100dB (typical 115dB)
  - 20Hz-20kHz: > 85dB (typical 95dB)
- Frequency response
  - 20Hz- 12kHz :  $\pm$  0.1dB max
  - 12kHz-20kHz :  $\pm$  0.2dB max
- Signal to noise ratio : > 95dB (typical 100 dB)
- Dynamic range
  - 1kHz : > 90dB
  - 20Hz-20kHz : > 88dB
- Distortion and noise:
  - 1kHz : > 85dB(typical 89 dB)
  - 20Hz-20kHz : > 80dB(typical 89 dB)
- Intermodulation distortion : > 87dB
- Phase non linearity :  $\pm$  1° max.
- Level non linearity :  $\pm$  0.5dB max.
- Mute (spin-up, pause, access) : >100dB
- Outband attenuation : > 50dB above 25kHz

#### Headphone output (only DVD930)

30mW at 32 Ohm load.

Headphone impedance: 8-2000 Ohm

### Video performance

#### SCART

For Europe version only

Pin signals :

- Output Audio R : 1.8V RMS
  - Output Audio L : 1.8V RMS
  - Audio GND
  - Blue GND
  - Blue : 0.7Vpp  $\pm$  0.1V into 75 Ohm (\*)
  - function switching :
    - 2V TV
    - >4.5V / <7V asp. ratio 16:9 DVD
    - >9.5V / <12V asp. ratio 4:3 DVD
  - Green GND
  - Output Green : 0.7Vpp  $\pm$  0.1V into 75 Ohm (\*)
  - Red GND
  - Output red : 0.7Vpp  $\pm$  0.1V into 75 Ohm (\*)
  - fast switching RGB/ CVBS :
    - <0.4V into 75 Ohm = CVBS
    - >1V / <3V into 75 Ohm = RGB
  - CVBS GND
  - fast switching GND
  - Output CVBS/RGB sync:
    - 1Vpp  $\pm$  0.1v into 75 Ohm
  - Shield
  - 2,6,10,12,14,20 not connected
- (\*) for 100% white

### CVBS

Video output : 1 Vpp  $\pm$  0.1V into 75 Ohm

#### S Video

For USA version only

Output Y : 1 Vpp  $\pm$  0.1V into 75 Ohm

Output C : burst 300 mVpp +/-4dB into 75 Ohm

### Video format

#### Digital compression :

MPEG 2 for DVD  
MPEG 1 for VCD

#### DVD

	50 Hz	60Hz
Horizontal Resolution :	720 pixels	720 pixels
Vertical Resolution :	576 lines	480 lines

#### VCD

Horizontal Resolution :	352 pixels	352 pixels
Vertical Resolution :	288 lines	240 lines

### Digital output

CDDA/ LPCM: according IEC958  
MPEG1, MPEG2, AC3: according IEC1937

### Dimensions and weight

Apparatus tray closed : WxDxH :435 x 305 x 70/83  
Apparatus tray open : WxDxH:435 x 423 x 70/83  
Weight without packaging : ca. 4 Kg  
Weight in packaging : ca. 6 Kg

### Optical read-out system

Laser type : Semiconductor AlGaAs  
Output power : < 5 mW(3mW typical)  
Wavelength : 650 nm  
Numerical Aperture : 0.60(DVD)  
0.45(VCD/CD)

## DIAGNOSTIC SOFTWARE : SCRIPT INTERFACES

### DEALER SCRIPT

The dealer script can give a diagnosis on a standalone DVD player; no other equipment is needed to perform a number of hardware tests to check if the DVD player is faulty.

A Diagnostic Nucleus is a part of the Diagnostic Software. Each nucleus contains an atomic and software independent diagnostic test, testing a functional part of the DVD player hardware. These nuclei are described in chapter: "Description of Diagnostic Nuclei"

The order in which the nuclei are called are not of interest to the user. The ordering for the nuclei will be done according to the different modules of the DVD player:

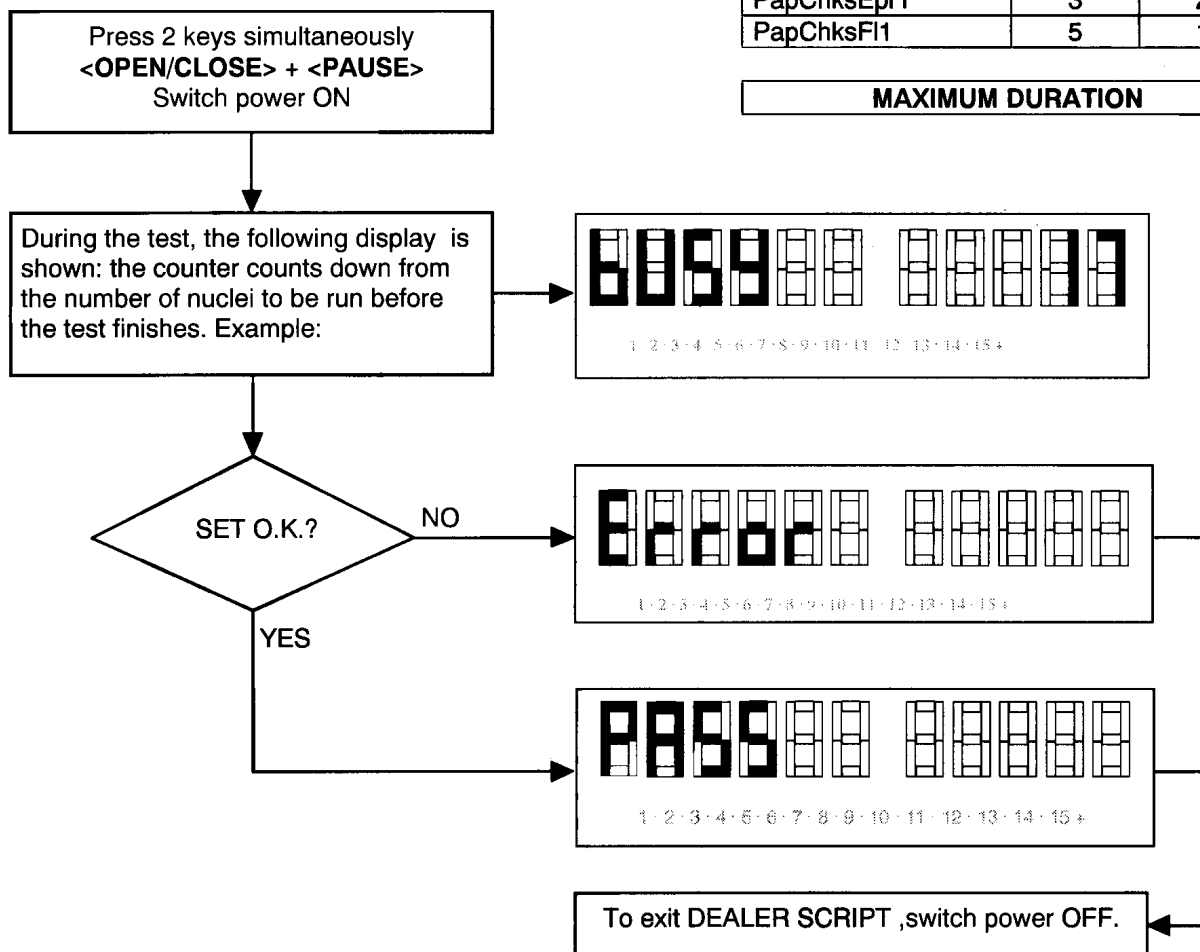
Nuclei will only be part of the dealer script if they are meaningful on a standalone DVD player (without tv set or other equipment attached).

The nuclei called in the dealer script are the following (the number after each nucleus name corresponds with the number being on the local display when the nucleus is executed during the dealer script):

**Remark : Although the Dealer script may result in PASS, it is possible that the set doesn't output sound or picture because the A/V MUX board hasn't been tested during this script.**

Nucleus	Nucleus Number	Number on display	Duration
VideoColDsmOn	37a	23	3-6 sec
VideoColDsmOff	37b	22	10 msec
CompDsmDvpAcc	22	21	100 msec
CompDsmDramWrR	25	20	11 sec
CompDvpFifoSig	23	19	100 msec
CompLsiAcc	63	18	100 msec
CompLsiDramAcc	65	17	100 msec
CompLsiDramWrR	64	16	210 sec
PapDramWrR	13	15	12 sec
PapI2cCtrl	15	14	10 msec
PapI2cDenc	19	13	100 msec
PapI2cDisp	17	12	50 msec
PapI2cMca	69	11	100 msec
PapI2cNvram	16	10	10 msec
VideoSigLsiOn	67a	9	100 msec
VideoSigLsiOff	67b	8	10 msec
PapS2bEcho	20	7	3-8 sec
PapIntDsm	8	6	100 msec
PapIntDvp	9	5	100 msec
PapIntI2c	7	4	100 msec
PapIntLsi	66	3	100 msec
PapChksEpr1	3	2	2 sec
PapChksFl1	5	1	2 sec

<b>MAXIMUM DURATION</b>	<b>252 sec</b>
-------------------------	----------------



## PLAYER SCRIPT

### Purpose of Player Script

The Player script will give the opportunity to perform a test which will determine which of the DVD player's modules are faulty, to read the error log and error bits and to perform an endurance loop test. To successfully perform the tests, the DVD player must be connected to a tv set (PAL or Multistandard) to check the output of a number of nuclei.

To be able to check results of certain nuclei, the player script expects some interaction of the user (e.g. to approve a test picture or a test sound). Some nuclei (i.e. nuclei that test functionality of the Basic Engine module) require that the DVD player itself is opened, to enable the user to observe moving parts and approve their movement visually.

Only tests within the scope of the diagnostic software will be executed hence only faults within this scope can be detected.

### Contents of Player Script

The player script contains all nuclei that are useful on a DVD player which is connected to a tv-set and help to determine which module of the DVD player is faulty, as well as to read out the contents of the error logs.

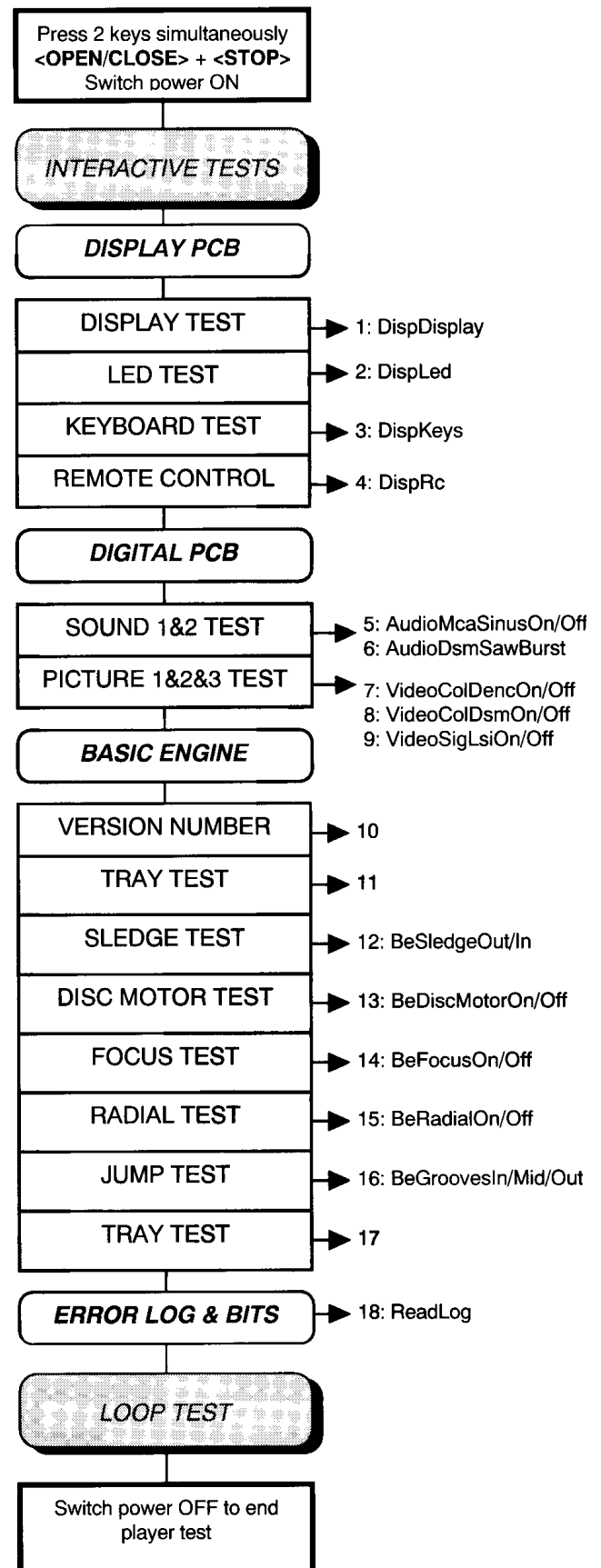
### Structure of Player Script

The player script consists of a set of nuclei testing the three hardware modules in the DVD player: the Display PCB, the Digital PCB and the Basic Engine.

Reading the error log and error bits information can be useful to determine any errors that occurred recently during normal operation of the DVD player.

The loop test will perform the same nuclei as the dealer test, but it will loop through the list of nuclei indefinitely.

### Survey



# INTERACTIVE TESTS

## DISPLAY PCB

### : DISPLAY TEST

The display test is performed by nucleus DispDisplay. By putting a series of test patterns on the local display, the local display is tested. To step through all different patterns, the user must either press PLAY (pattern is ok) or PAUSE (pattern was incorrect) to proceed to the next pattern. The display of patterns is continued in a cyclic manner until the user presses NEXT.

Note that a different example picture is used here to show all different display patterns. All other examples in this document are simplified for essentials.

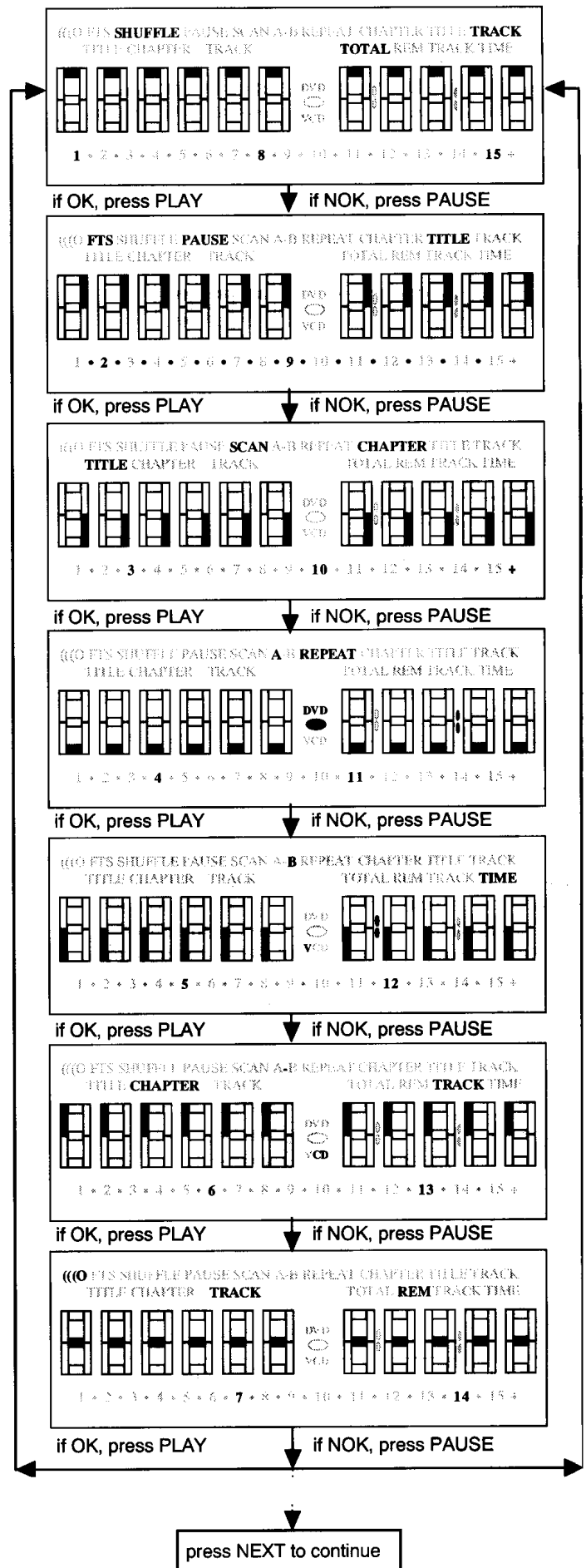
If the user presses NEXT before all display patterns are tested, the DispDisplay nucleus will return FALSE and cause an error in the overall result of the player script.

### : LED TEST

The LED on the DVD player is tested by nucleus DispLed.

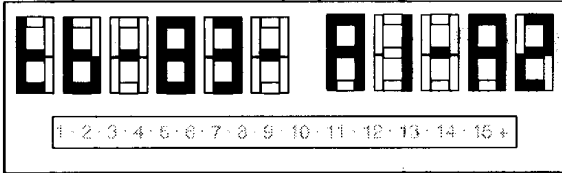
The user must check if the LED is lighted; if it is, press PLAY, if it is not lit up press PAUSE. By pressing NEXT the script will proceed to the next test.

If the user presses NEXT before PLAY or PAUSE, the DispLed nucleus will return FALSE and cause an error in the overall result of the player script.



## 2.3 KEYBOARD TEST

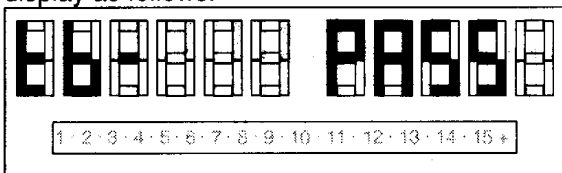
The keyboard of the DVD player is tested by nucleus DispKeys. The user is expected to press all keys on the local keyboard once. The code of the key pressed is shown on the local display (1 hexadecimal digit) immediately followed by a (hexadecimal) number indicating how many times that key has been pressed. Example of the local display during this test:



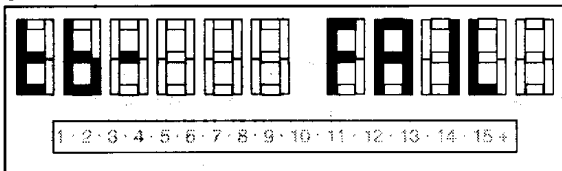
The key-codes displayed on the local display will scroll from right to left when the display gets full, the text "tb-" will remain on display.

key id.	key
0	PLAY
1	NEXT
2	PREVIOUS
3	PAUSE
4	STOP
5	REPEAT
6	FTS
7	SCAN
8	BACKWARD
9	OPEN / CLOSE
A	FORWARD
b	SHUFFLE

If any keys are detected more than once (due to hardware error), the key-code is displayed twice (or more), with the second digit increased by 1. If the user does not press all keys minimally once (in any order), the DispKeys nucleus will return FALSE and cause an error in the overall result of the player script. The user can leave the keyboard test by pressing the NEXT key on the local display of the DVD player for at least one full second. The result of the keyboard test is shown on local display as follows:



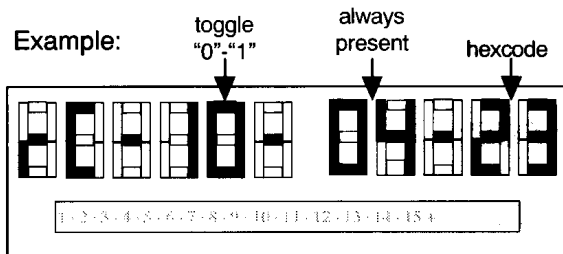
or



Pressing NEXT on the local keyboard again will proceed to the next test.

## REMOTE CONTROL TEST

The remote control of the DVD player is tested by nucleus DispRc. The user must press any key on the remote control just once. The codes of the key pressed will be shown on the local display in hexadecimal format as long as the key will be kept pressed.

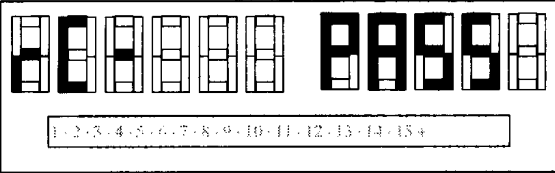


The user can leave the remote-control test by pressing NEXT on the local keyboard of the DVD player. The remote control test is successful if a code was received before the user pressed the NEXT key; pressing the NEXT key before pressing a key on the remote control gives an error in the remote control test (note that the remote control test will also fail if a key on the remote control was pressed but no code was received). The remote control test does not check upon the contents of the received code, i.e. it will not be checked if the received code matches the key pressed. If desired, the user can manually check this code by using a code-table for the remote control key-codes.

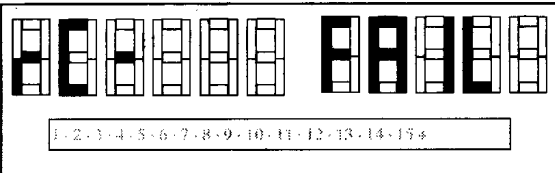
RC Key id	Hexadecimal code
STANDBY	C
STOP	31
PLAY	2C
PLAY BACKWARD	2d
PAUSE	30
STEP FORWARD	F6
STEP BACKWARD	F5
FORWARD	22
FORWARD 4X	dF
FORWARD 8X	E0
BACKWARD	29
BACKWARD 4X	dE
BACKWARD 8X	dd
SLOW	22
SLOW 2	d8
SLOW BACKWARD	23
SLOW BACKWARD 2	db
NEXT	20
PREVIOUS	21
CURSOR UP	58
CURSOR DOWN	59
CURSOR LEFT	5A
CURSOR RIGHT	5b
OK	5C
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
TOGGLE	C8
ANGLE	85
AUDIO	4E
SUBTITLES	4b
SUBTITLE ON/OFF	E3
ROOT MENU	54
TITLE MENU	71
MENU	d1
SETUP MENU	82
OSD ON/OFF	F
RETURN	83
RESUME	d7

SCAN	2A
SHUFFLE	1C
REPEAT	1d
A/B REPEAT	3b
TOGGLE SCART	43
OPEN/CLOSE	42
FTS	Fb

After pressing NEXT, the result of the remote control test is displayed on the local display of the DVD player as follows:



or

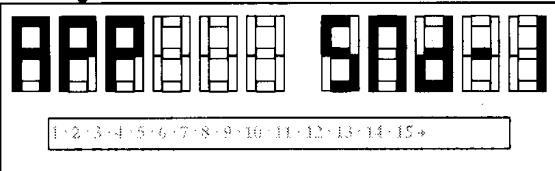


Pressing NEXT on the local keyboard again will proceed to the next test.

## DIGITAL PCB

### : SOUND 1 TEST

The first soundtest is performed by starting a sinus sound which needs confirmation from the user (nucleus AudioMcaSinusOn); the display will show the following message:

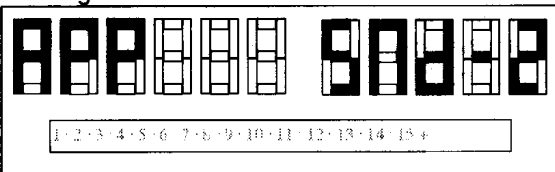


By pressing PLAY the user confirms the test(reset of the sinus sound with a call to nucleus AudioMcaSinusOff); pressing PAUSE will indicate the sound was inaudible or incorrect.

Pressing NEXT will proceed to the next test if the user presses NEXT without pressing PLAY or PAUSE first, the result of this test will be FALSE.

### : SOUND 2 TEST

The second soundtest is performed by starting a sawtooth sound of 50 Hz during 3 seconds (nucleus AudioDsmSawBurst); the display will show the following message:

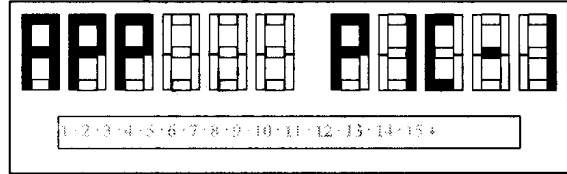


By pressing PLAY the user confirms the test, pressing PAUSE will indicate the sound was inaudible or incorrect.

Pressing NEXT will proceed to the next test if the user presses NEXT without pressing PLAY or PAUSE first, the result of this test will be FALSE

### 2.7 : PICTURE 1 TEST

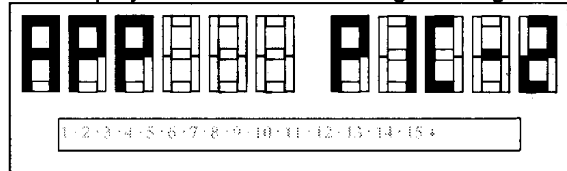
The first displaytest is performed by putting a predefined picture on the display (nucleus VideoColDencOn) and asking the user for confirmation. The display will show the following message:



By pressing PLAY the user confirms the test, pressing PAUSE will indicate the picture was invisible or incorrect. Pressing NEXT will proceed to the next test (after a reset of the picture on display by calling VideoColDencOff); if the user presses NEXT without pressing PLAY or PAUSE first, the result of this test will be FALSE.

### : PICTURE 2 TEST

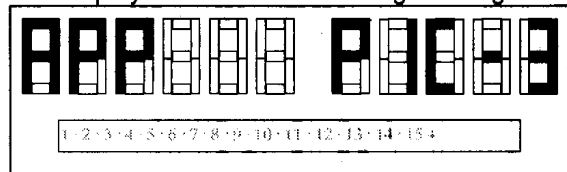
The second displaytest is performed by putting a predefined picture on the display (nucleus VideoColDsmOn) and asking the user for confirmation. The display will show the following message:



By pressing PLAY the user confirms the test, pressing PAUSE will indicate the picture was invisible or incorrect. Pressing NEXT will proceed to the next test (after a reset of the picture on display by calling VideoColDsmOff); if the user presses NEXT without pressing PLAY or PAUSE first, the result of this test will be FALSE.

### PICTURE 3 TEST

The third displaytest is performed by putting a predefined picture on the display (nucleus VideoSigLsiOn) and asking the user for confirmation. The display will show the following message:

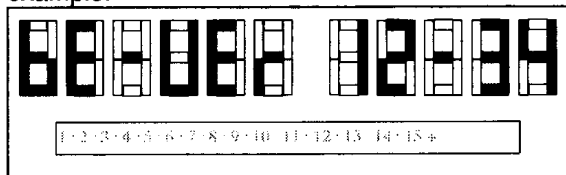


By pressing PLAY the user confirms the test, pressing PAUSE will indicate the picture was invisible or incorrect. Pressing NEXT will proceed to the next test (after a reset of the picture on display by calling VideoSigLsiOff); if the user presses NEXT without pressing PLAY or PAUSE first, the result of this test will be FALSE.

## BASIC ENGINE

### : VERSION NUMBER

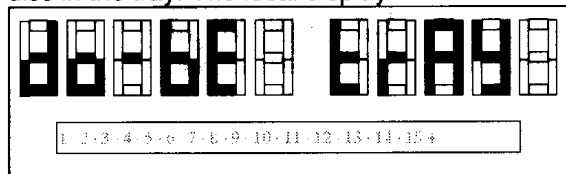
In the basic engine tests, the version number of the Basic Engine will be shown first, as the following example:



By pressing the NEXT key, the Basic Engine tests are started.

### : TRAY TEST

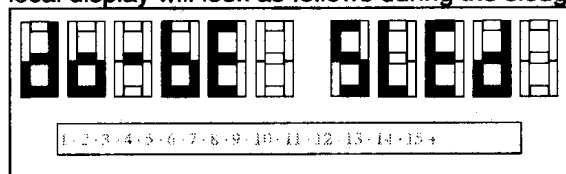
First, the tray is tested. The purpose of this test is also to give the user the opportunity to put a disc in the tray of the DVD player. Some tests on the Basic Engine require that a disc (e.g. DVD MPTD test disc) is present in the player. At the end of the Basic Engine tests this tray test will be repeated solely to enable the user to remove the disc in the tray. The local display will look as follows:



By pressing PLAY or PAUSE the user can toggle the position of the tray. The user should close the tray at the end of this test. Note that this test will not contribute to the test result of the Basic Engine. Pressing NEXT will proceed to the next test.

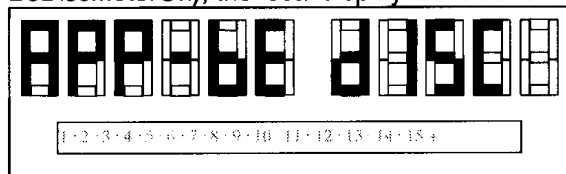
### : SLEDGE TEST(listening test)

The second Basic Engine test tests the sledge; the user can move the sledge as many times as desired by using PLAY (nucleus BeSledgeOut) and PAUSE (nucleus BeSledgeIn). Pressing NEXT on the local keyboard proceeds to the next test. Note that this test will not contribute to the test result of the Basic Engine. The local display will look as follows during the sledge test:



### : DISC MOTOR TEST(visual test)

The third Basic Engine test tests the disc motor (nucleus BeDiscMotorOn); the local display looks as follows:

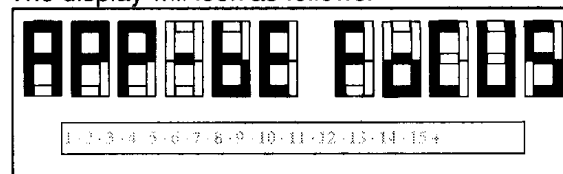


By pressing PLAY the user confirms that the disc motor is running; pressing PAUSE indicates the disc motor does not work. Pressing NEXT proceeds to the next test, after a reset of the disc motor (nucleus BeDiscMotorOff).

If the user presses NEXT before pressing PLAY or PAUSE, the result of this test will be FALSE.

### : FOCUS TEST(listening test)

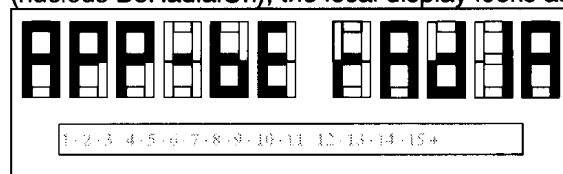
The fourth Basic Engine test tests the focussing; first focussing is turned on by calling nucleus BeFocusOn. The display will look as follows:



By pressing PLAY the user confirms that the focussing was successful; pressing PAUSE indicates a focussing failure. Pressing NEXT proceeds to the next test after a reset of the focussing (nucleus BeFocusOff); if NEXT is pressed before PLAY or PAUSE, the result of this test will be false.

### : RADIAL TEST(visual & listening test)

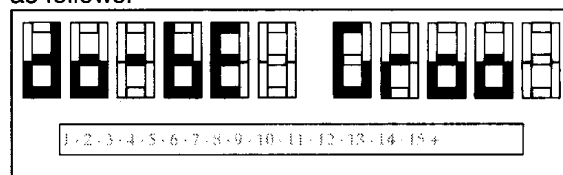
The fifth Basic Engine test tests the radial functionality (nucleus BeRadialOn); the local display looks as follows:



By pressing PLAY the user confirms that the radial function worked; pressing PAUSE indicates the function does not work. Pressing NEXT proceeds to the next test, after a reset of the radial (nucleus BeRadialOff). If the user presses NEXT before pressing PLAY or PAUSE, the result of this test will be FALSE.

### : JUMP TEST(listening test)

The sixth and last Basic Engine test tests the jumping by calling nuclei BeGroovesIn, BeGroovesMid and BeGroovesOut. During this test, the local display looks as follows:

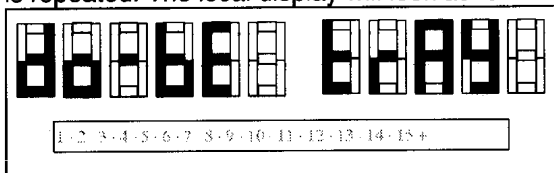


The user can switch between the three different types of groove settings by pressing PLAY (forward to next nucleus in the list In-Mid-Out) or PAUSE (backward in the list In-Mid-Out). This is done in a cyclic manner; note that this test will not contribute to the test result of the Basic Engine. Pressing NEXT proceeds to the next test, after the disc motor has been shut off with a call to nucleus BeDiscMotorOff.



### 2.17 : TRAY TEST

As a last action for the Basic Engine tests, the tray test is repeated. The local display will look as follows:

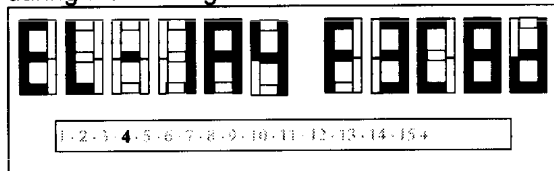


This test is meant to give the user the opportunity to remove the disc in the tray. The tray position can be toggled using the PLAY and PAUSE key. The user must close the tray before proceeding to the next test with the NEXT key.

### Error Log and Error Bits

#### : ERROR LOG

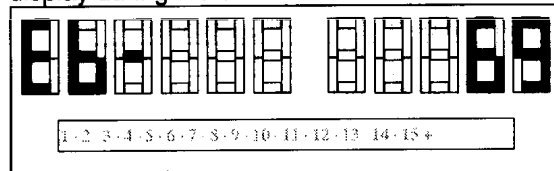
Reading the error log and error bits information can be useful to determine any errors that occurred recently during normal operation of the DVD player. Reading the error log is done by nucleus ReadLog. The display during the errorlog readout looks as follows :



By pressing PLAY or PAUSE the user can move forward or backward (respectively) through the logged error codes. The highlighted number indicates which errorcode is currently on display (in the example above, errorcode number 4 is displayed). If "0000" is displayed at all positions, the error log is empty. Display of the logged errors is done in a cyclic manner. The errorcode with the lowest highlighted number is the most recent. By pressing NEXT on the local keyboard, the user can proceed to the next test.

#### : ERROR BITS

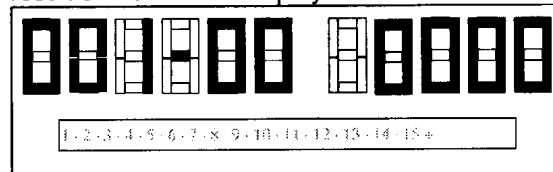
Reading the error bits is done by nucleus ReadBits. The display during the errorbits readout looks as follows:



Only the set errorbits will be shown by their (decimal) number. Refer to the appropriate documentation for the explanation of each bit number. If the display only shows "EB-0", no error bits were set. By pressing NEXT the user can continue to the next test.

### LOOP TEST

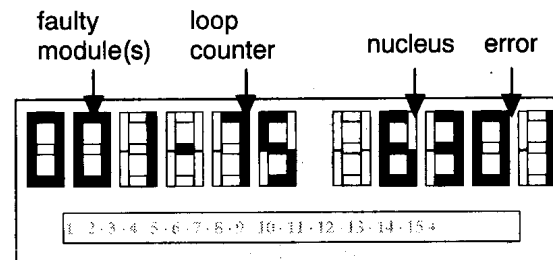
At the start of the loop test, the display will show the result of the interactive player test:



The left side of the display contains a 3-digit code, which can have a value between 000 and 111. These values are to be interpreted as follows:

Displayed Value	Indication for each module		
	Basic Engine	Digital PCB	Display PCB
000	ok	ok	ok
001	ok	ok	faulty
010	ok	faulty	ok
011	ok	faulty	faulty
100	faulty	ok	ok
101	faulty	ok	faulty
110	faulty	faulty	ok
111	faulty	faulty	faulty

The loop test will perform the same nuclei as the dealer test, but it will loop through the list of nuclei indefinitely. The display of the DVD player will display not only the three digits indicating correct/faulty modules and the last found error code (as mentioned, faults are detected as far as they can be within the scope of the diagnostic software), but also a loop counter indicating how many times the loop has been gone through. Example:

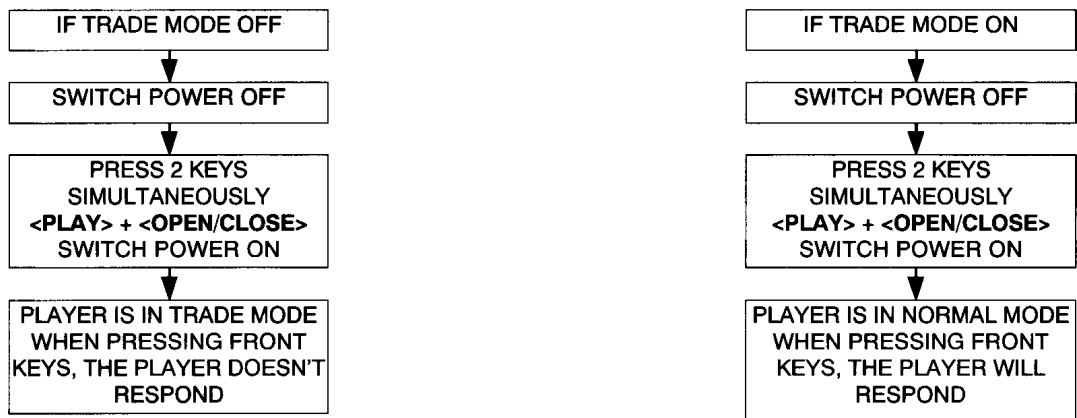


The number after the hyphen indicates the number of times the loop test has been performed; the 4 digits at the right side of the display show the last error that was found when running the loop test: the leftmost two digits of this code indicate which nucleus resulted in a fault; the rightmost two digits refer to the faultcode within that nucleus. For further explanation of this error code, see list of error codes on next page.

## ERROR CODES LOOP TEST

<b>ERROR CODE</b>	<b>NUCLEUS NUMBER</b>	<b>ERROR DESCRIPTION</b>
0301	3	Calculated checksum of EPROM1 is not correct
0501	5	Calculated checksum of FLASH1 is not correct
0701	7	I2C interrupt active before start
0702		I2C interrupt not activated
0703		I2C interrupt not de-activated
0704		I2C interrupt byte send time-out
0705		I2C bus busy before start
0801	8	DSM interrupt active before start
0802		DSM interrupt not activated
0803		DSM interrupt not de-activated
0901	9	DVP interrupt active before start
0902		DVP interrupt not activated
0903		DVP interrupt not de-activated
1301	13	The DVD DRAM is faulty
1501	15	I2C access error
1601	16	I2C bus busy before start
1602		NVRAM access time-out
1603		No NVRAM Acknowledge
1604		NVRAM reply time-out
1701	17	I2C bus SLAVE uP busy
1702		I2C bus not working
1703		Slave controller not responding
1704		Slave response is not correct
1901	19	I2C bus DENC busy before start
1902		DENC access time-out
1903		DENC access error
1904		DENC read time-out
2001	20	Parity error from basic engine to serial
2002		Parity error from serial to basic engine
2003		No communication between serial and basic engine
2004		Communication time-out error
2201	22	Address line AX is not connected to the DSM/DVP
2202		Data line DX is not connected to the DSM/DVP
2301	23	The FIFO connected to the DVP or its interconnections are faulty
2302		A time-out occurred while waiting for the signature calculation of the DVP
2501	25	The DSM DRAM is faulty
3701	37a	The signature is faulty
3702		A time-out occurred while waiting for the signature calculation by the DVP
3703		DENC not responding
6301	63	Dataline of the LSI MPEG decoder is not connected. Or one or more address lines are stuck-at.
6401	64	A time-out occurred during a read/write operation to the DRAM of the LSI MPEG decoder
6402		DRAM chip nr XXXX of the LSI MPEG decoder is faulty.
6501	65	A time-out occurred during the access to the DRAM of the LSI MPEG decoder
6502		Data line of DRAM is stuck-at.
6503		Address line of DRAM is stuck-at.
6504		Address line of DRAM is not connected.
6701	67a	The signature is wrong
6702		A time-out occurred while waiting for the signature calculation of the DVP.
6901	69	MCA access failure

## TRADE MODE



## Servicing DVD module and Digital board

The DVD module(Basic Engine) and the digital board will be exchanged completely in case of failure. The defective modules and boards have to be returned to a central repairshop.

### Reprogramming of new digital boards.

#### Caution

***This information is confidential and may not be distributed. Only a qualified service person should reprogram the digital board.***

After replacement of the digital board, all the customer settings and also the region code will be lost. Reprogramming of the digital board will put the player back in the state in which it has left the factory, i.e. with the default settings and the allowed region code.

Reprogramming will be done by way of the remote control.

Put the player in stop mode, no disc loaded.

Press the following keys on the remote control:

<PLAY> followed by numerical keys <2> <7> <4>

The display shows: “- - - - -”

Press now successively the following keys :

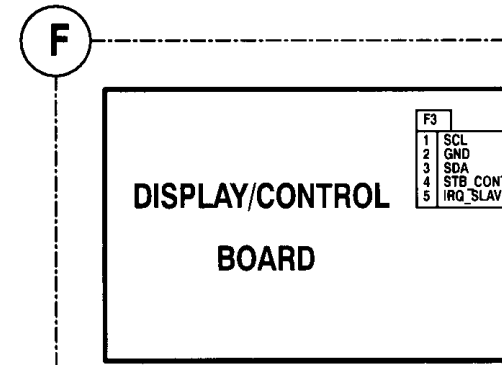
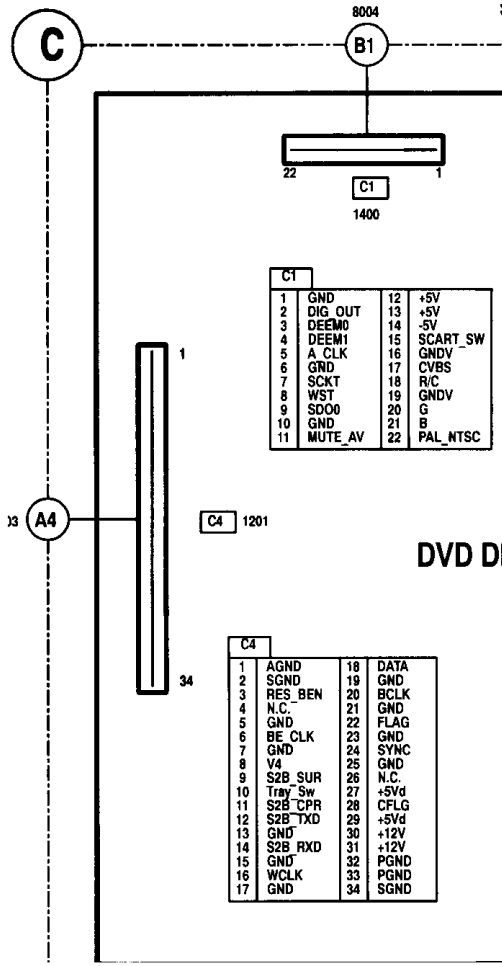
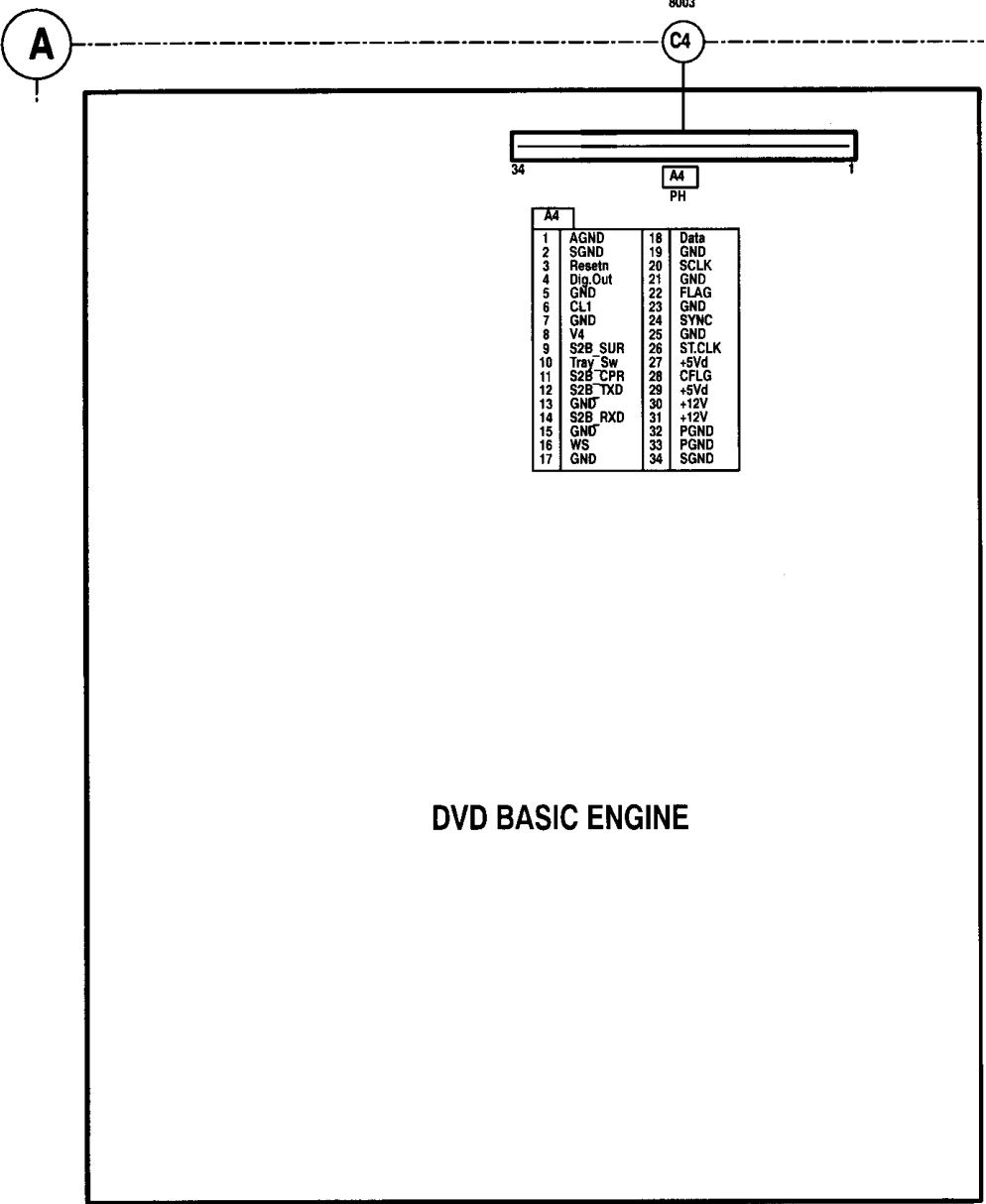
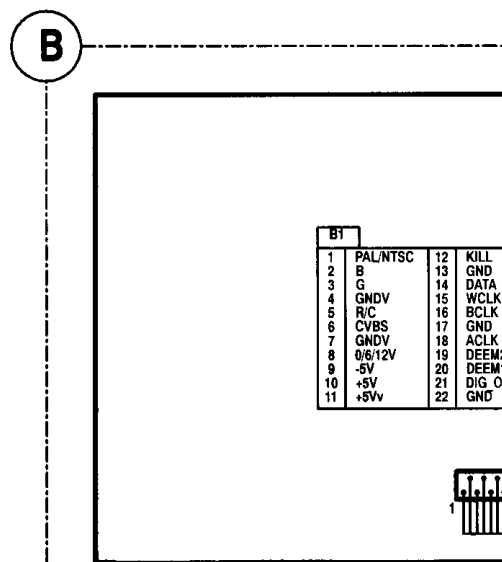
for DVD730 : <0><0><1><0><0><0><1><2><8><1><5><6>

for DVD930 : <0><0><2><0><0><0><1><2><8><1><5><6>

Press <PLAY> again.

The TV screen will become **red** during a short time to confirm that the digital board has been reprogrammed.

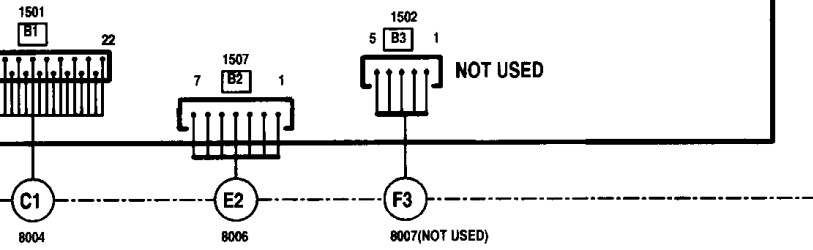
WIRING DIAGRAM



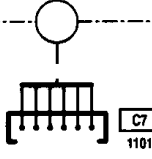
# A/V MUX BOARD

B2	
1	AUDL
2	GND A
3	AUDR
4	+5VA
5	MICRO
6	GND A
7	-5V

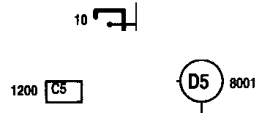
B3	
1	K Reset
2	K CLK
3	GND
4	K Data
5	K Strobe



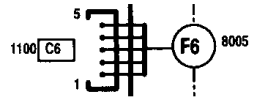
# SERVICE SERIAL INTERFACE



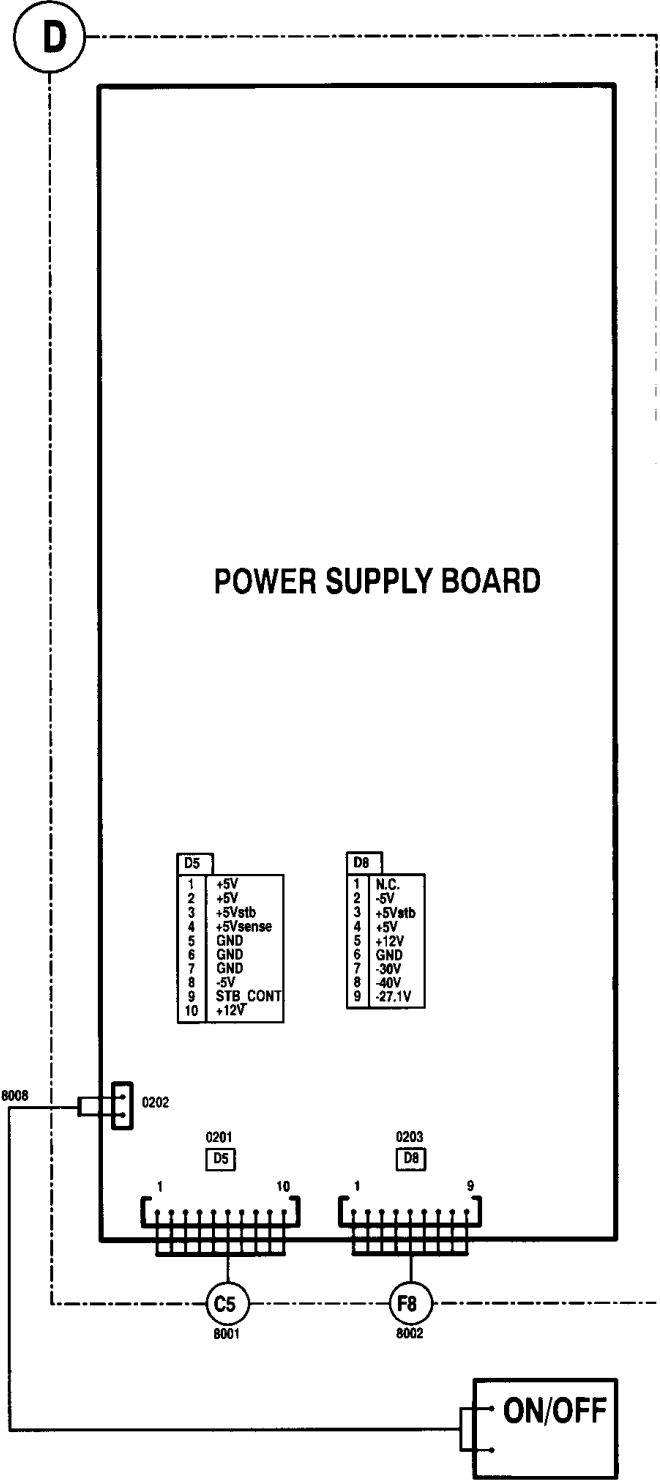
C5	
1	+5VA
2	+5V
3	+5Vstb
4	+5Vsense
5	GND A
6	PGND
7	-5V
8	STB_CONT
9	+12V
10	



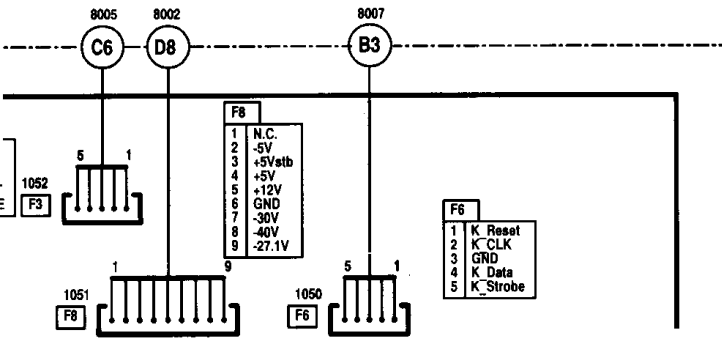
C6	
1	SCL
2	GND
3	SDA
4	STB_CONT
5	IRQ_SLAVE



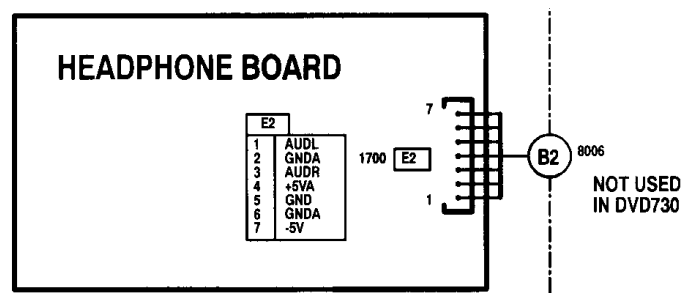
# DIGITAL BOARD



# NOT USED

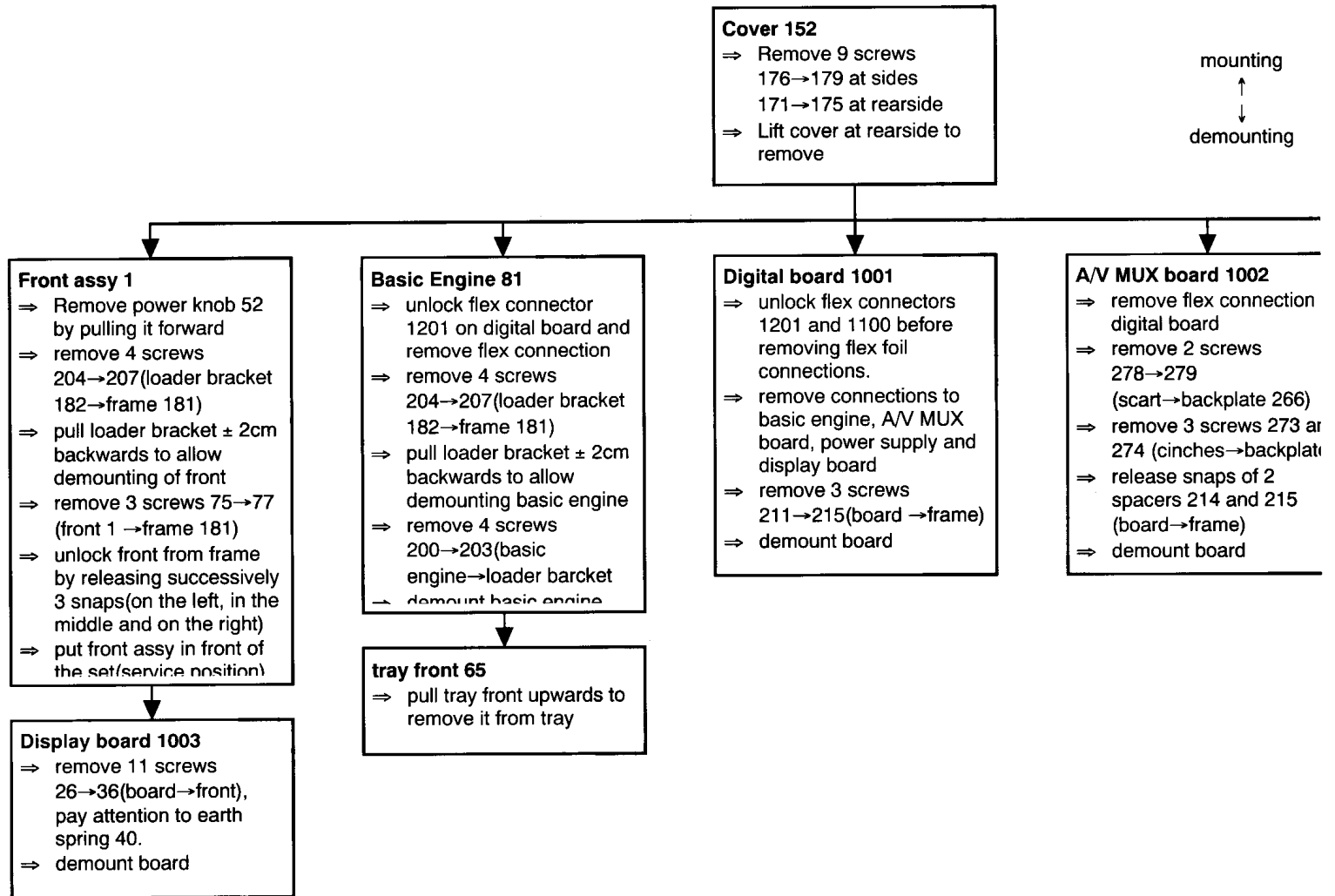


# E



## DISMANTLING INSTRUCTIONS DVD730

See exploded view for item numbers



## MECHANICAL PARTSLIST

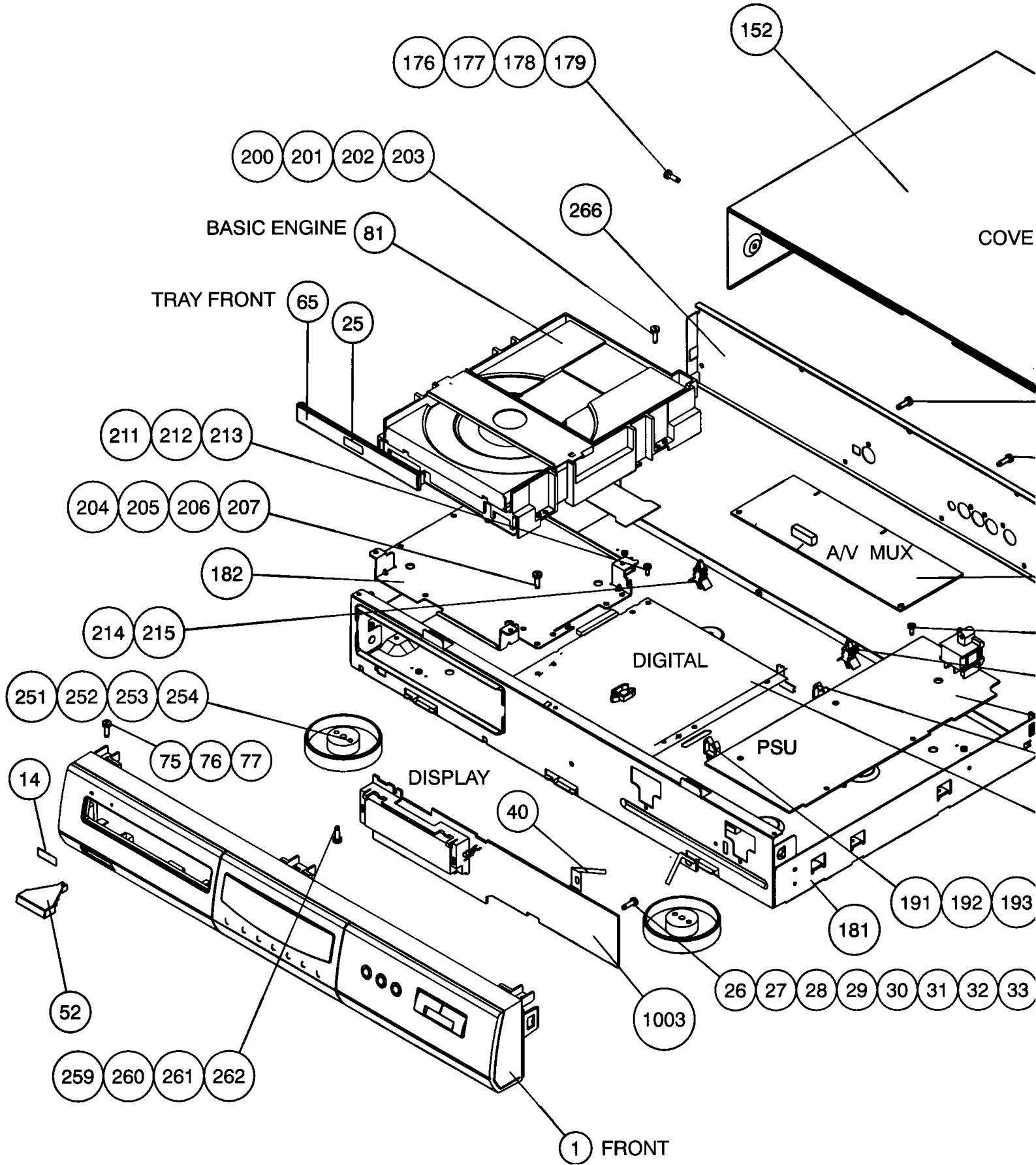
1	4822 459 04838	FRONT ASSY
14	4822 459 10887	WORDMARK
25	4822 454 13252	DVD LOGO
52	4822 410 11551	POWERKNOB
65	4822 459 04843	TRAY FRONT
81	4822 214 12599	DVD MODULE PACKED
251	4822 462 42159	FOOT SILVER
252	4822 462 42159	FOOT SILVER
253	4822 462 42159	FOOT SILVER
254	4822 462 42159	FOOT SILVER
301	4822 321 10249	SBC1201 MAINS CABLE
314	4822 321 61847	SCART CABLE
318	4822 219 10405	REMOTE CONTROL RC1501/01
1001	4822 214 12608	DIGITAL BOARD 4169



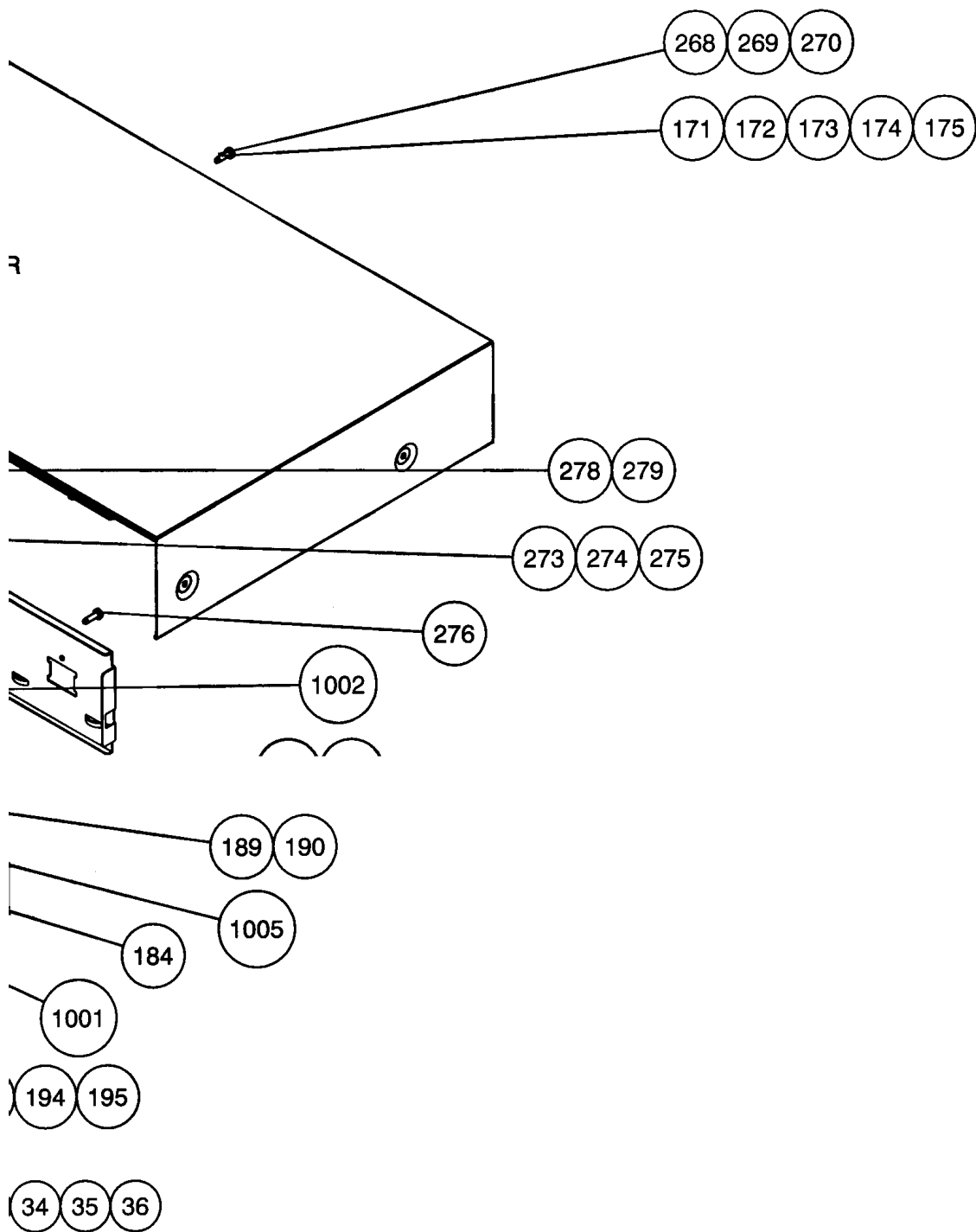
**Power supply unit 1005**

- ⇒ remove connections
- ⇒ remove 2 screws 209 and 210(board→frame)
- ⇒ remove screw 276 (mains inled→backplate)
- ⇒ release snaps of spacers 189 and 190 (board→frame)
- ⇒ demount board

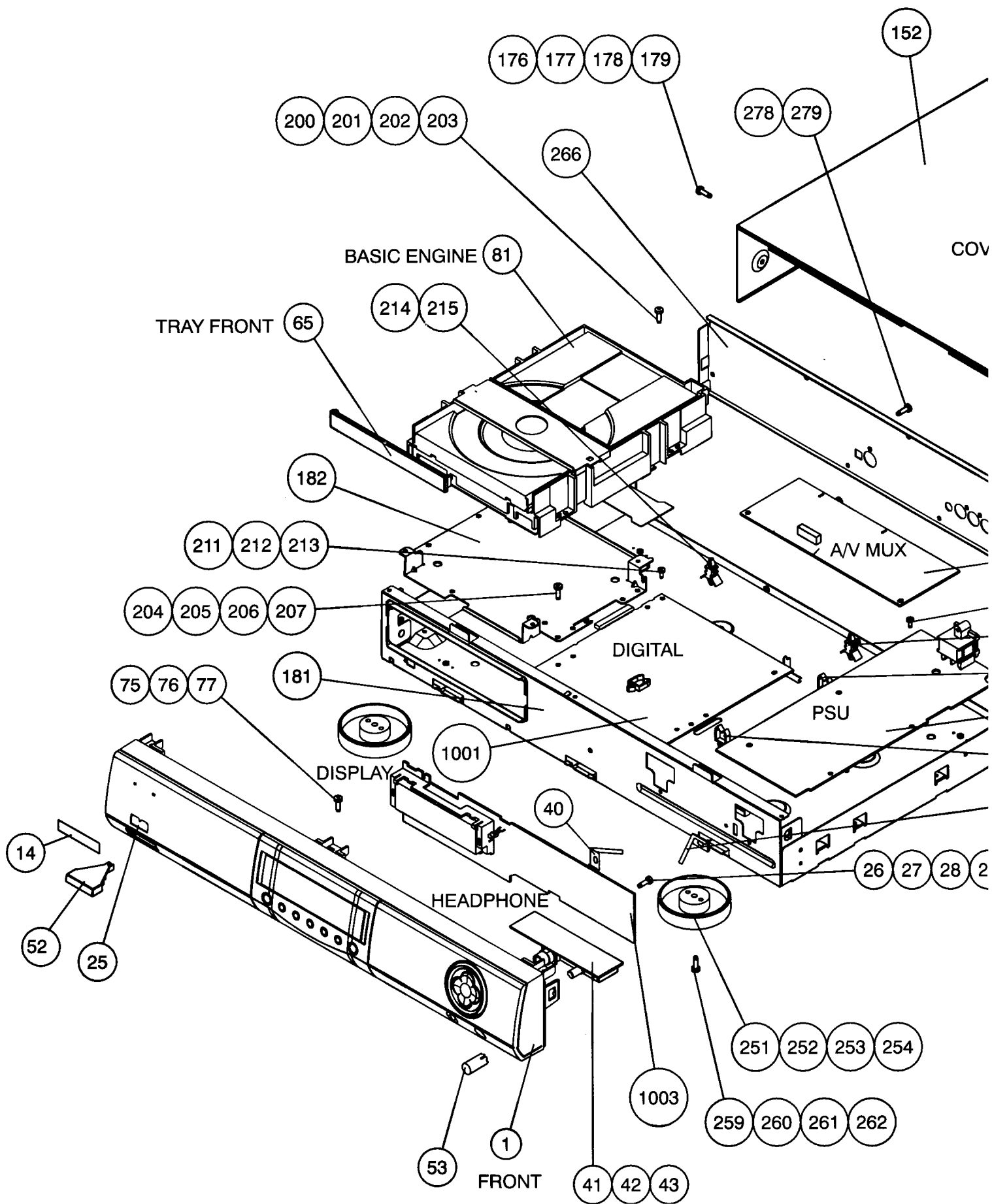
EXPLODED VIEW DVD730

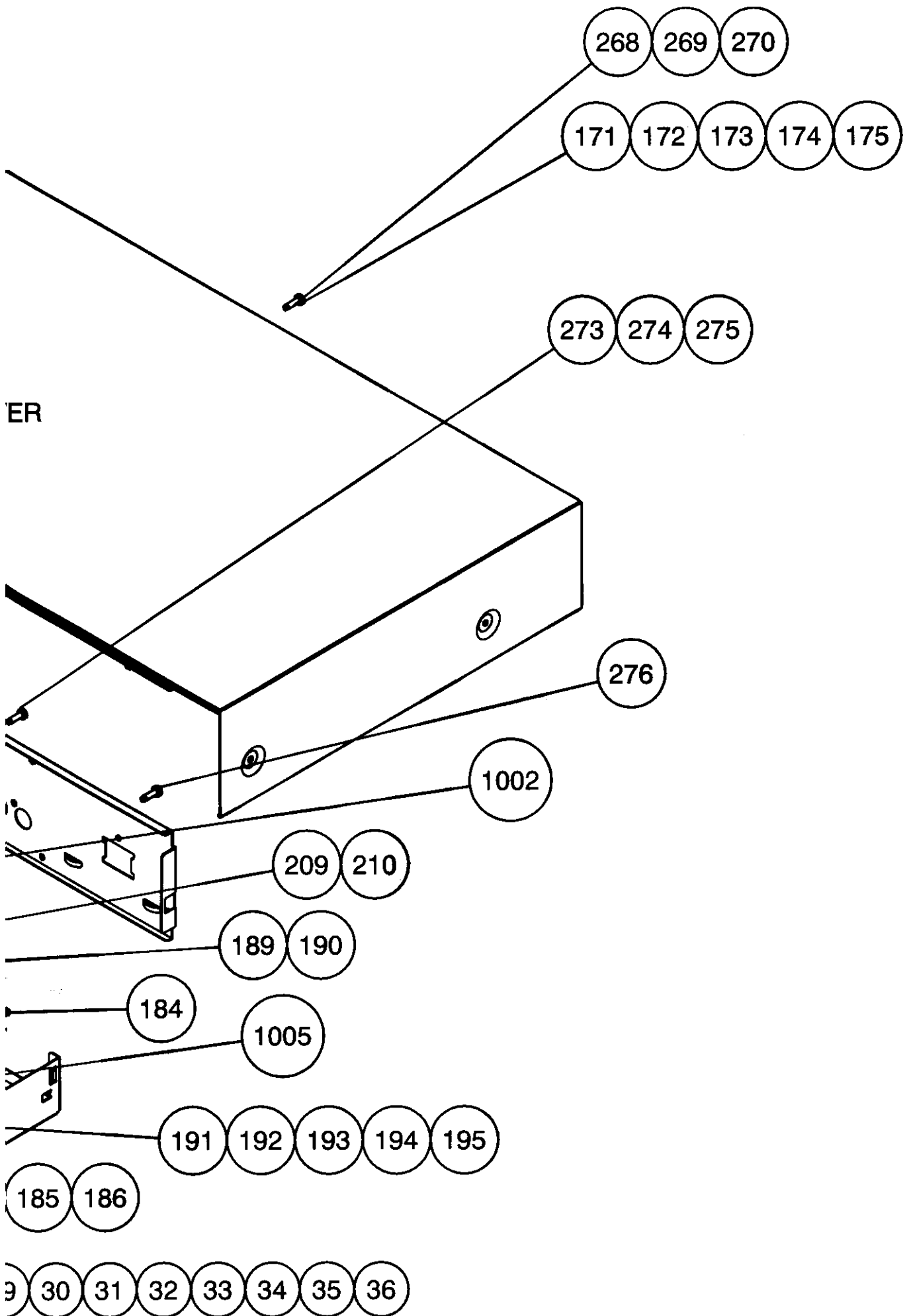






EXPLODED VIEW DVD930





**DISMANTLING INSTRUCTIONS DVD930**

See exploded view for item numbers

**Cover 152**  
 ⇒ Remove 9 screws  
 176→179 at sides  
 171→175 at rearside  
 ⇒ Lift cover at rearside to remove

**Front assy 1**  
 ⇒ Remove power knob 52  
 by pulling it forward  
 ⇒ remove 3 screws 75→77  
 (front 1 →frame 181)  
 ⇒ unlock front from frame  
 by releasing successively  
 3 snaps(on the left, in the  
 middle and on the right)  
 ⇒ put front assy in front of  
 the set(service position)

**Basic Engine 81**  
 ⇒ unlock flex connector  
 1201 on digital board and  
 remove flex connection  
 ⇒ remove 4 screws  
 200→203(basic  
 engine→loader barcket  
 ⇒ demount basic engine

**tray front 65**  
 ⇒ pull tray front upwards to  
 remove it from tray

**Digital board 1001**  
 ⇒ unlock flex connectors  
 1201 and 1100 before  
 removing flex foil  
 connections.  
 ⇒ remove connections to  
 basic engine, A/V MUX  
 board, power supply and  
 display board  
 ⇒ remove 3 screws  
 211→215(board →frame)  
 ⇒ demount board

**A/V MUX board**  
 ⇒ remove flex  
 digital board  
 ⇒ remove 2 s  
 278→279  
 (scart→bac  
 ⇒ remove 3 s  
 274 (cinch  
 ⇒ release sna  
 spacers 21  
 (board→fra  
 ⇒ demount b

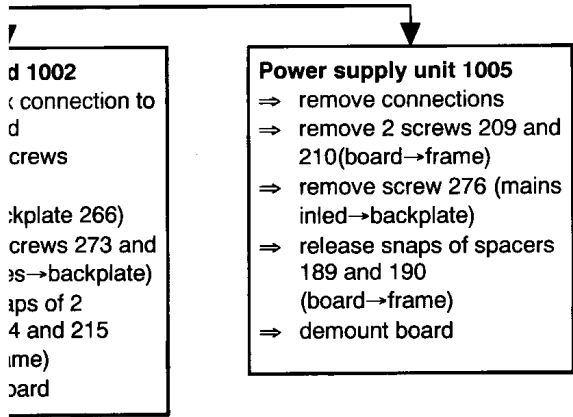
**Display board 1003**  
 ⇒ remove 11 screws  
 26→36(board→front),  
 pay attention to earth  
 spring 40.  
 ⇒ demount board

**Headphone board 1003**  
 ⇒ remove volume knob  
 53 by pulling it  
 forward  
 ⇒ remove 3 screws  
 41→43(board→front)  
 ⇒ demount board

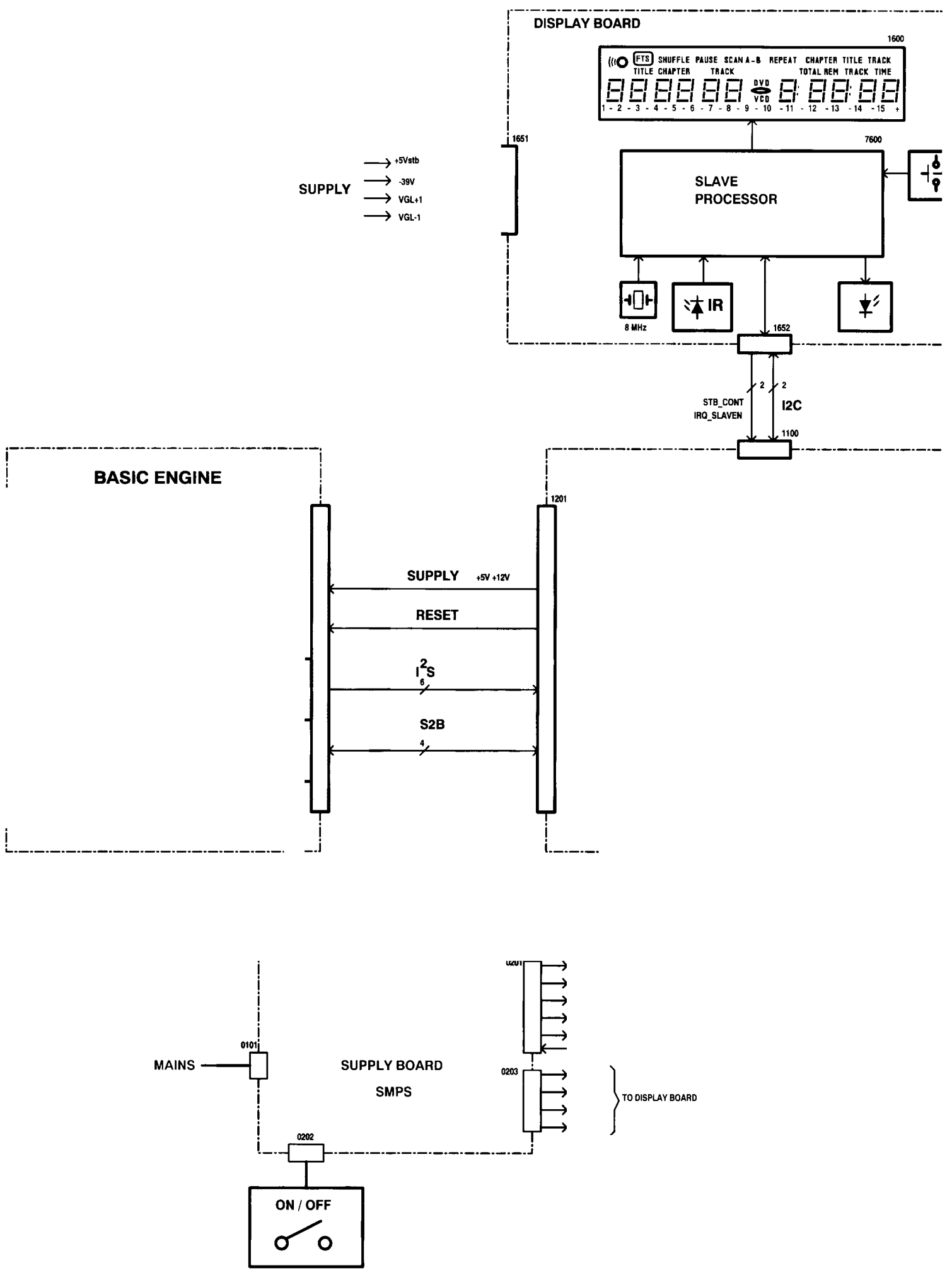
**MECHANICAL PARTSLIST**

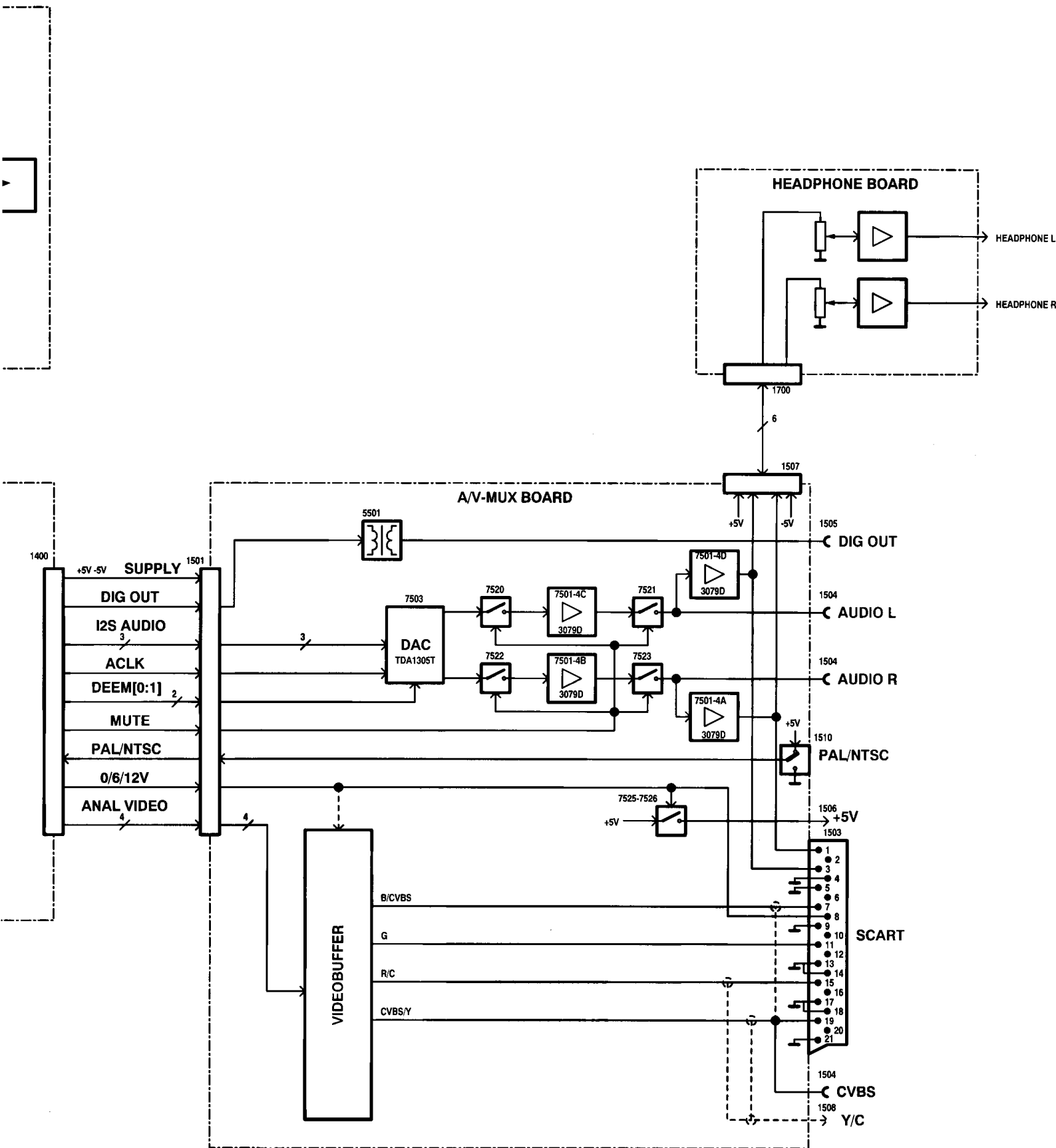
1	4822 459 04837	FRONT ASSY
14	4822 459 10887	WORDMARK
24	4822 454 13251	MATCHLINE LOGO
25	4822 454 13252	DVD LOGO
52	4822 410 11551	POWERKNOB
53	4822 410 10284	KNOB VOLUME
65	4822 459 04844	TRAY FRONT
81	4822 214 12599	DVD MODULE PACKED
251	4822 462 42159	FOOT SILVER
252	4822 462 42159	FOOT SILVER
253	4822 462 42159	FOOT SILVER
254	4822 462 42159	FOOT SILVER
301	4822 321 10249	SBC1201 MAINS CABLE
313	4822 321 11357	AUDIO CORD SET
314	4822 321 61847	SCART CABLE
316	4822 321 61579	VIDEO CORD (CINCH PLUG)
318	4822 219 10404	REMOTE CONTROL RC8401/01
1001	4822 214 12608	DIGITAL BOARD 4169

mounting  
↑  
↓  
mounting



# OVERALL BLOCKDIAGRAM





## **SIGNALS & ABBREVIATIONS**

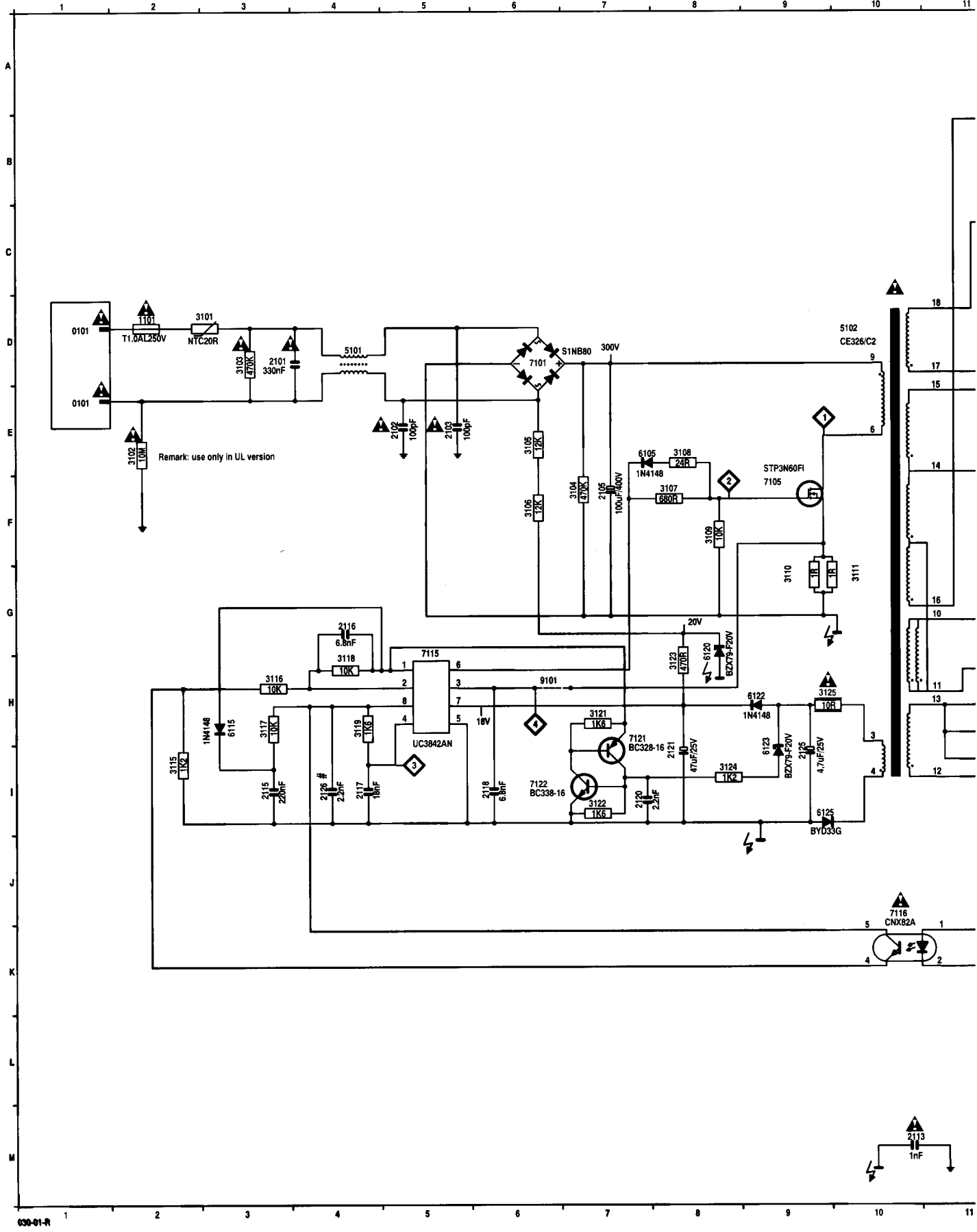
13M5_CLK	external clock 13.5 MHz for Digital Signal Processor
27M_CLK	external clock 27MHz for Programmable Logic Device
27M_DENC	external video clock 27MHz for video encoder
27M_DSM	external video clock 27MHz for DVD Stream Manager
27M_FIFO	external video clock 27MHz for FIFO
27M_LSI	external video clock 27MHz for MPEG decoder
3M68_CLK	external clock 3.680 MHz for Host Processor
40M_CLK	external clock 40 MHz
6M75_CLK	I2C bus clock 6.75 MHz
90K_CLK	Host interface DSM: Clock 90 kHz out
A[0:23]	System Address bus
A_BCLK	Serial audio bit clock
A_CLK	External audio clock for DVD Stream Manager, Digital Signal Processor and Audio DAC.
A_CSZ	Audio channel zero start
A_DATA	Serial audio data
A_WCLK	Audio word select
AO[1:9]D	Address bus from DRAM controller to DRAM
AS_COMPN	address strobe DRAM controller
ASN	Address strobe
BA[0:8]	address bus Mpeg decoder → Drams
BD[0:63]	data bus Mpeg decoder → Drams
BE_CLK	Basic Engine clock
CASN	Column Address Strobe
CLK1M	Host interface DSM 1 MHz clock out
CLKOUT	Clock output 32.768kHz of Host Processor
CS_DSMN	Chip select for DVD Stream Manager
CS_DVPN	Chip select for DVD Digital Video Postprocessor
CS_I2CN	Chip select for I2C processor
CS_LSI	Chip select for MPEG decoder
CS0N	Chip select control signal 0
CS1N	Chip select control signal 1
CS2N	Chip select control signal 2
CTS1P	Clear to send control line of Serial Interface
D[0:15]	System Data bus
DEEM0	Deemphasis control signal 0
DEEM1	Deemphasis control signal 1
DIG_OUT	Digital Audio Data
DMA_ACK	DMA acknowledge
DMA_DONE	DMA ready
DMA_REQN	DMA request
DSACK0N	Data strobe aknowledge control signal 0
DSACK1N	Data strobe aknowledge control signal 1
DSN	Data Strobe
DSN2	Data Strobe
DTACK_DRCN	Data acknowledge DRAM controller
DTACK_I2CN	Data Acknowledge I2C-BUS CONTROLLER
EPROM_CE0N	EPROM memory chip enable control signal 0
EPROM_CE1N	EPROM memory chip enable control signal 1
FLASH_CE0N	FLASH memory chip enable control signal 0
FLASH_CE1N	FLASH memory chip enable control signal1
HS	Horizontal Synchronization
IRQ_DSMN	Interrupt request DVD Stream Manager
IRQ_DVPN	Interrupt request DVD Digital Video Postprocessor
IRQ_I2CN	Interrupt request I2C Processor
IRQ_LSI	Interrupt request MPEG decoder
IRQ_SLAVEN	Interrupt request SLAVE Processor
IRQ3N	Interrupt request control signal 3
IRQ5N	Interrupt request control signal 5
IRQ6N	Interrupt request control signal 6
LCAS1ND	Lower column address strobe 1
LCAS2ND	Lower column address strobe 2
LDS_DRCN	Lower column address strobe DRAM controller
MODCK	Modify clock

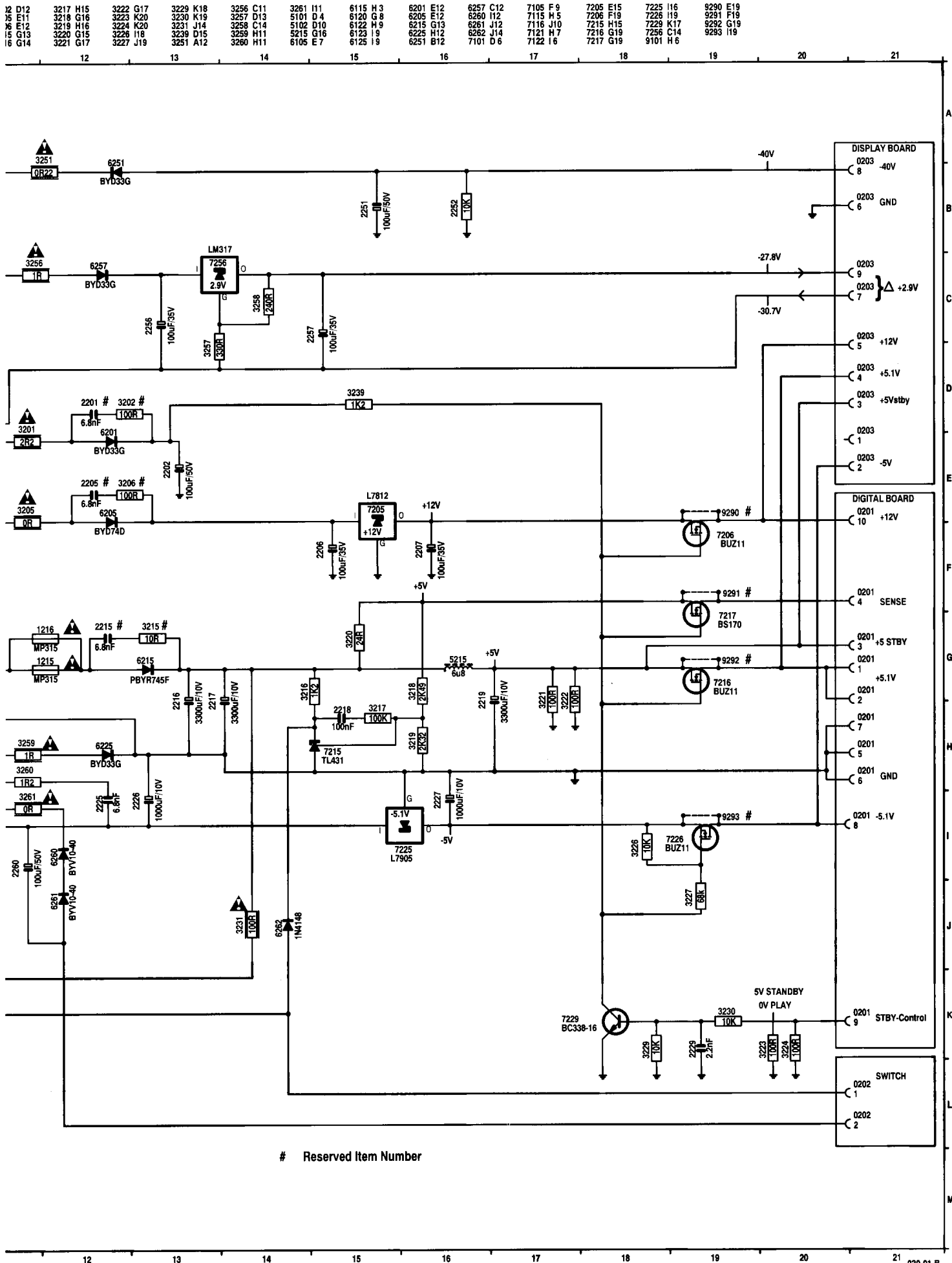


MUTE	Mute control signal
MUTE_AV	Mute Audio/Video control signal
MUTE_EN	Mute enable control signal
OEN	Output Enable
OEND	Output enable DRAM
PAL_NTSC	PAL/NTSC switch
RAS1ND	Row address strobe 1
RAS2ND	Row address strobe 2
RASN	Row Address Strobe
RES_BEN	Reset for Basic Engine
RES_DSP	Reset for Digital Signal Processor
RES_LSIN	Reset for MPEG decoder
RESET_PLS	Reset for Programmable logic device
RESETN	Hard reset
RNW	Read(LOW) or Write(HIGH) control signal
RTSEX	Request to send control line of Serial Interface
RWN	Read(HIGH) or Write(LOW)
RX1P	Receive data port of Serial Interface
S_BS	Sub picture byte sync
S_DATA	Sub picture data
S_REQN	Sub picture request
S_ST	Sub picture start
S2B_CPR	Serial to Basic interface : Control Processor Ready to accept data
S2B_RXD	Serial to Basic interface : Receive data
S2B_SUR	Serial to Basic interface : Servo Unit Ready to accept data
S2B_TXD	Serial to Basic interface : Transmit data
SCART_SW	Scart Switch control signal
SCART0	Scart control signal 0
SCART1	Scart control signal 1
SCKT	Transmit serial clock
SCL	I2C bus clock
SDA	I2C bus data
SDO0	Transmit serial data output0
SEL_ACLK	Select Audio clock
SIZ0	Size: indicates the number of bytes remaining to be transferred for this cycle.
STB_CONT	Standby control
TCK_TAP	Boundary scan test clock
TDI_TAP	Boundary scan test data input
TDO_DSM	Boundary scan test data output from DVD Stream Manager
TDO_LSI	Boundary scan test data output from MPEG decoder
TDO_TAP	Boundary scan test data output
TMS_TAP	Boundary scan test mode select
TRST_TAP	Boundary scan test reset
TX1P	Transmit data port of Serial Interface
UCAS1ND	Upper column address strobe 1 DRAM
UCAS2ND	Upper column address strobe 2 DRAM
UDS_DRCN	Upper column address strobe DRAM controller
V_DATA	Serial video data
V_REQN	Video data request
V_SCLK	Video Serial Clock
V_VVAL	Video valid
VS_DVP	Vertical synchronization Digital Video Postprocessor
VS_MPEG	Vertical synchronization MPEG decoder
WAITN	Data wait
WEN	Write Enable
WEND	Write enable DRAM
WST	Transmit word select output
YUV_DVP[0:7]	Luminance and Chrominance signal Digital Video Postprocessor
YUV_MPEG[0:7]	Luminance and Chrominance signal MPEG decoder

POWER SUPPLY CIRCUIT DIAGRAM

0101 E 1	0201 F21	0201 K21	0203 E21	0203 C21	1216 G12	2113 M10	2120 I7	2202 E13	2216 G13	2226 I12	2256 C13	3103 D3	3108 E8	3116 H3	3122 I7	32
0101 D 1	0201 H21	0201 E21	0203 D21	0203 B21	2101 D3	2115 I3	2121 I8	2205 E12	2217 G13	2227 I16	2257 C14	3104 F7	3109 F8	3117 H3	3123 H8	32
0201 G21	0201 H21	0202 L21	0203 D21	0203 C21	2102 E5	2116 G4	2125 I9	2206 F15	2218 H15	2229 K19	2260 I11	3105 E6	3110 G9	3118 H4	3124 I8	32
0201 G21	0201 H21	0202 L21	0203 D21	1101 D 2	2103 E5	2117 I4	2126 I4	2207 F16	2219 G16	2251 B15	3101 D3	3106 F6	3111 G10	3119 H4	3125 H9	32
0201 G21	0201 I21	0203 E21	0203 B21	1215 G12	2106 F7	2118 I6	2201 D12	2215 G12	2225 I12	2252 B16	3102 E2	3107 F8	3115 I2	3121 H7	3201 D11	32



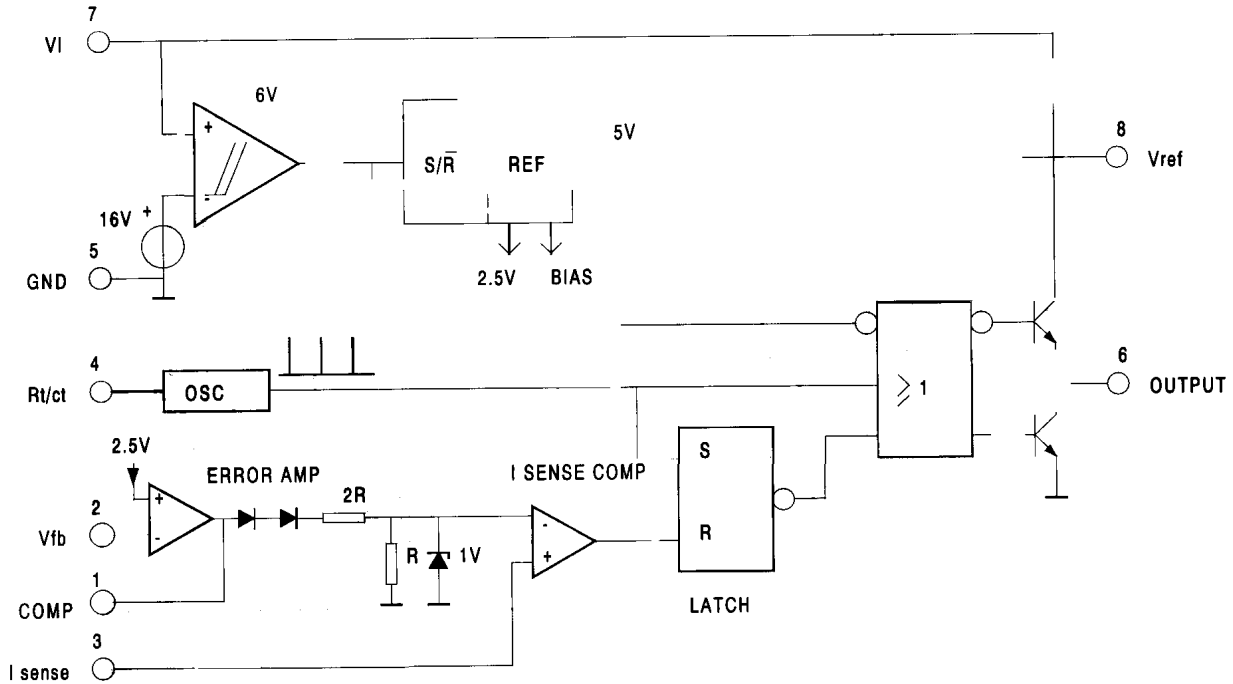


## Circuit description of the current mode power supply

### Function description

MOSFET 7105 is used as a power switch controlled by the current mode controller IC 7115. When the switch is closed, energy is transferred from the mains into the transformer. This energy is then supplied to the load when the switch is opened. By control of the switched-on time, the energy which is transferred in each cycle is regulated so that the output voltages are independent of load or input voltage variations. The controlling device UC3842 is an integrated pulse width modulator. A clock signal initiates power pulses at a fixed frequency. The termination of each output pulse occurs when an analogue of the inductor current reaches a threshold established by the error signal. In this way the error signal actually controls the peak inductor current.

### Description of UC3842



**Figure 1 : Blockdiagram UC3842**

The input voltage  $V_{cc}$  (pin 7) is monitored by a comparator with hysteresis, enabling the circuit at 16V and disabling the circuit below 10V. The error amplifier compares a voltage  $V_{fb}$  (pin 2) related to the output voltage of the power supply, with an internal 2.5V reference. The current sense comparator compares the output of the error amplifier with the switch current  $I_{sense}$  (pin 3) of the power supply. The output of the current sense comparator resets a latch, which is set every cycle by the oscillator. The output stage is a totem pole, capable of driving a MOSFET directly.

### Start-up sequence

#### t1: Charging the capacitor at $V_{cc}$

$C_{2121}$  connected to the  $V_{cc}$  pin 7 will be charged exponentially via a bleeder resistor  $R_{3123}$ . The output is switched off during  $t_1$ .

#### t2: Charging of output capacitors

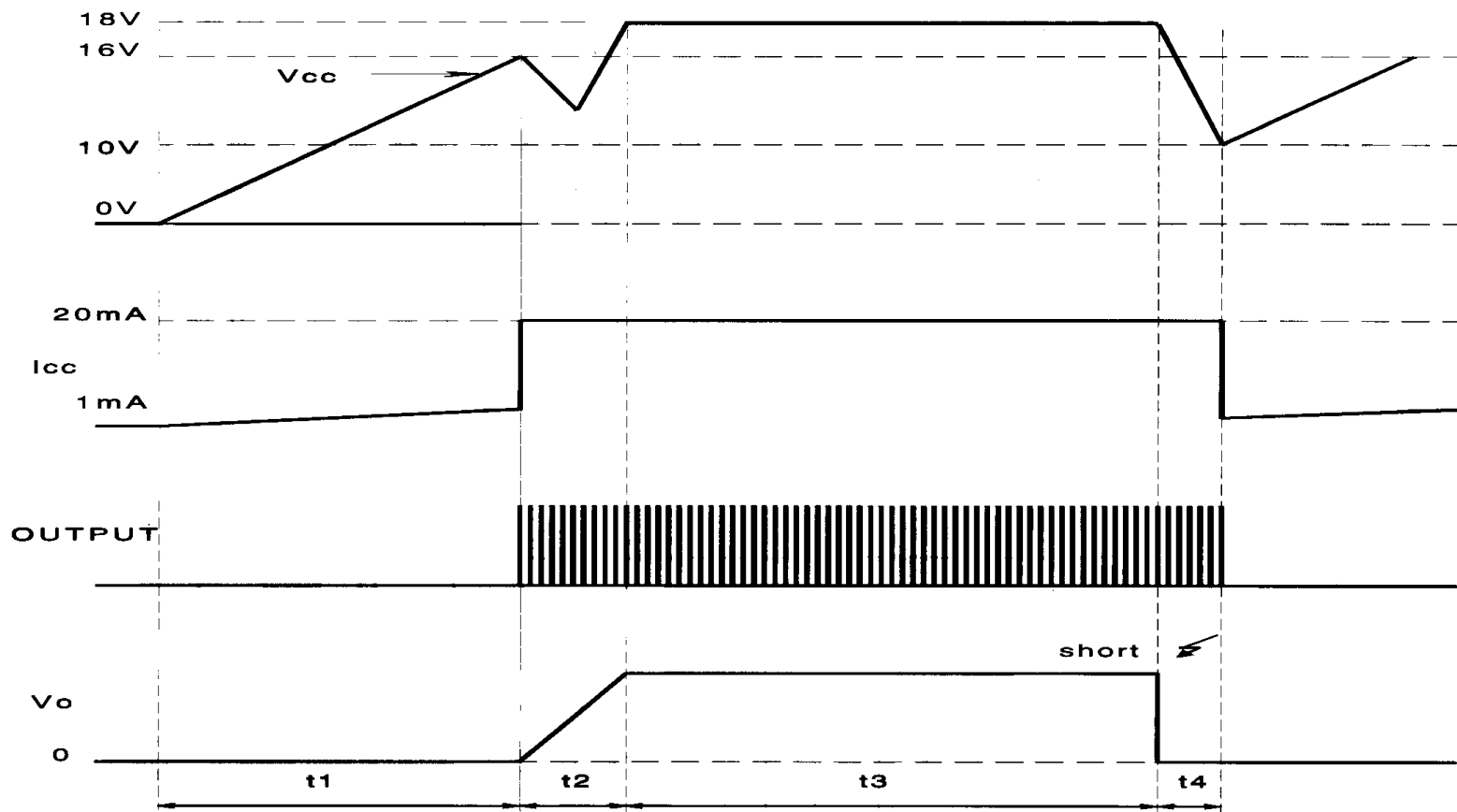
When the input voltage of the IC exceeds 16V, the circuit is enabled and starts to produce output pulses. The current consumption of the circuit increases to about 20mA, depending on the external loads of the IC. At first, the capacitor at the  $V_{cc}$  pin will discharge because the output capacitors of the power supply are still below the reflected  $V_{cc}$  voltage. At some moment during  $t_2$ ,  $V_{cc}$  reaches a minimum voltage, determined by the value of  $C_{2121}$ .

#### t3: regulation

The output voltage of the power supply is in regulation

#### t4: overload

When the output is shortened, the supply voltage of the circuit will decrease and after some time drop below the lower threshold voltage. At that moment, the output will be disabled and the process of charging the  $V_{cc}$  capacitor starts again. If the output is still shorted at the next  $t_2$  phase, the complete start-and stop sequence will repeat. The power supply comes in a hiccup mode.



**Figure 2: start-up sequenceRegulation**

Figure 3 shows the most relevant signals during the regulation phase of the power supply.

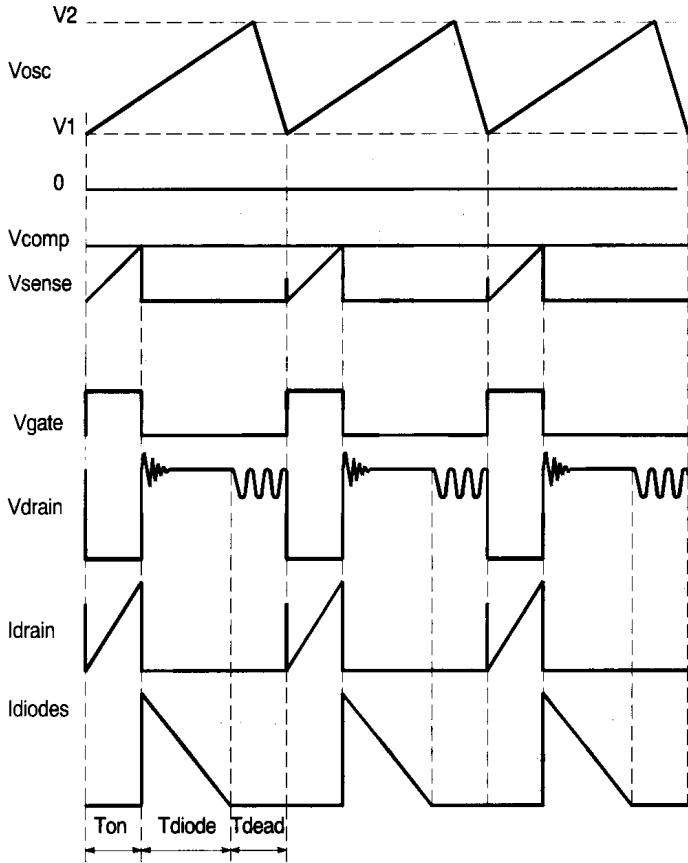
The oscillator voltage ramps up and down between  $V_1$  and  $V_2$ . The voltage at the current sense terminal is compared every cycle with the output of the error amplifier  $V_{comp}$ . The output is switched off when the current sense level exceeds the level at the output of the error amplifier.

1. **Time<sub>ON</sub> phase** : A drain current will flow from the positive supply at pin 9 through the transformer's primary winding, the MOSFET and  $R_{sense}$  to ground. As the positive voltage at pin 9 of the transformer is constant, the current will increase linearly and create a ramp dependent on the mains voltage and the inductance of the primary winding. A certain amount of energy is stored in the transformer in the form of a magnetic field. The polarity of the voltages at the secondary windings is such that the diodes are non-conducting.
2. **Time<sub>DIODE</sub> phase** : When the MOSFET is switched off, energy is no longer supplied to the transformer. The inductance of the transformer now tries to maintain the current which has been flowing through it at a constant level. The polarity of the voltage from the transformer therefore becomes reversed. This results in a current flow through the transformer's secondary winding via the diodes, electrolytic capacitors and the load. This current is also ramp shaped but decreasing.
3. **Time<sub>DEAD</sub> phase** : when the stored energy has been supplied to the load, the voltage from the secondary windings falls below the output voltage (held constant by the electrolytic capacitors) plus the threshold voltage of the diodes. The current in the secondary winding stops flowing. At this point, the drain voltage of the MOSFET is not yet zero because a certain charge is present between drain and source. This charge will start a sine-shaped ringing together with the transformer's self-induction.

The oscillator will start a next cycle which consists of the described three phases.

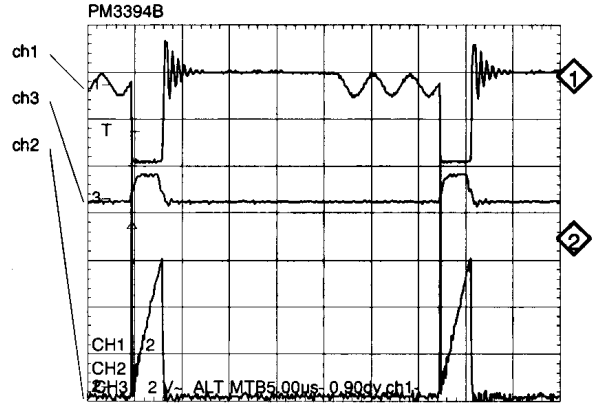
The time of the different phases depends on the mains voltage and the load.

Time<sub>DEAD</sub> is maximum at an input of 400V<sub>DC</sub> and minimum load, it will be zero at an input of 100V<sub>DC</sub> and overload.

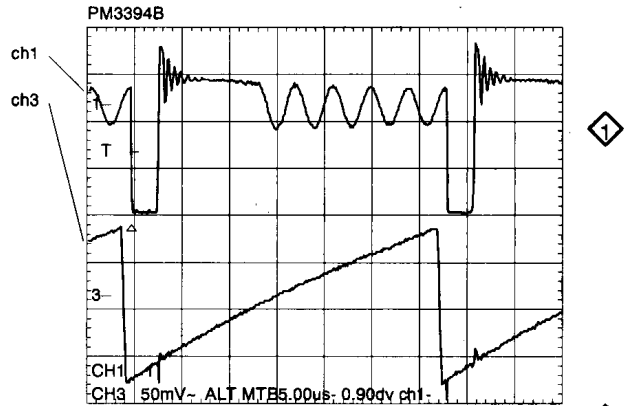


**Figure 3: Regulation**

**Oscillograms**



ch1 : Drain voltage  
 ch2 : Drain current  
 ch3 : Gate voltage



ch1 : Drain voltage  
 ch2 : Oscillator voltage at pin 4 of IC7115



ch1 : Drain voltage  
 ch3 : Sense voltage at pin 3 of IC7115

## Circuit description

### Input circuit

The input circuit consists of an EMI filter. The EMI filter is formed by L5101, C2101, C2102 and C2103. It prevents inflow of noises into/from the mains.

### Primary rectifier/smoothing circuit

The AC input is rectified by rectifier bridge 7101 and smoothed into C2105. The voltage over C2105 is approximately 300V. It can vary from 100V to 390V.

### Start circuit and Vcc supply

This circuit is formed by R3105, R3106, D6120, R3123, C2121, D6122, C2125, R3125, and D6125. When the power plug is connected to the mains voltage, the stabilised voltage over D6120(20V) will charge C2121 via R3123. When the voltage reaches 16V across C2121, the control circuit of IC7115 is turned on and the regulation starts. During regulation, Vcc of IC7115 will be supplied by the rectified voltage from winding 3-4 (D6122, C2121).

### Control circuit

The control circuit exists of IC7115, and its peripheral components. The frequency of the oscillator ( $\approx 30\text{kHz}$ ) is defined by R3119 and C2117.

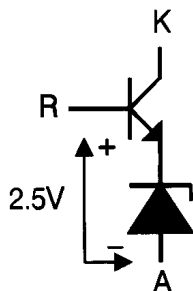
### Power switch circuit

This circuit comprises MOSFET 7105, Rsense 3110 and 3111.

### Regulation circuit

The regulation circuit comprises opto-coupler 7116 which isolates the error signal from the control IC on the primary side and a reference component 7215. The TL431(7215) can be represented by two components:

- a very stable and accurate reference diode
- a high gain amplifier



TL431 will conduct from cathode to anode when the reference is higher than the internal reference voltage of about 2.5V. If the reference voltage is lower, the cathode current is almost zero.

The cathode current flows through the LED of the opto-coupler. The collector current of the opto-coupler flows through R3115, producing an error voltage, connected to pin 2 of IC7612.

### Overvoltage protection circuit

This circuit consist of transistors 7121 and 7122, zenerdiode 6123, R3124, C2120, R3121 and R3122. When the regulation circuit is interrupted due to an error in the control loop, the +5V output voltage will increase (overvoltage). This overvoltage is sensed on the primary winding 3-4. When the rectified voltage over C2125 becomes higher than 20V, transistors 7121 and 7122 will conduct and the voltage on pin 1 of IC7115 will relapse. This results in a switching off of the drain current of MOSFET 7105. C2121 discharges until 10V. The process of charging and discharging C2121 will start (hiccup mode), establishing a safe situation.

### On/off circuit

This circuit is formed by R3261, C2260, D6260 and 6261, and an ON/OFF switch. When the switch is open the supply is ON, when closed, a negative voltage is fed to the opto-coupler interrupting the regulation circuit. This results in a switching off of the drain current of MOSFET 7105. The supply is OFF.

### Secondary rectifier/smoothing circuit

There are six rectifier/smoothing circuits on the secondary side. Each voltage depends on the number of windings of the transformer.

The +5V is used as supply voltage for the regulation loop.

The SENSE input serves as reference for the reference component 7215 thus compensating the losses caused by the wiring to the boards.

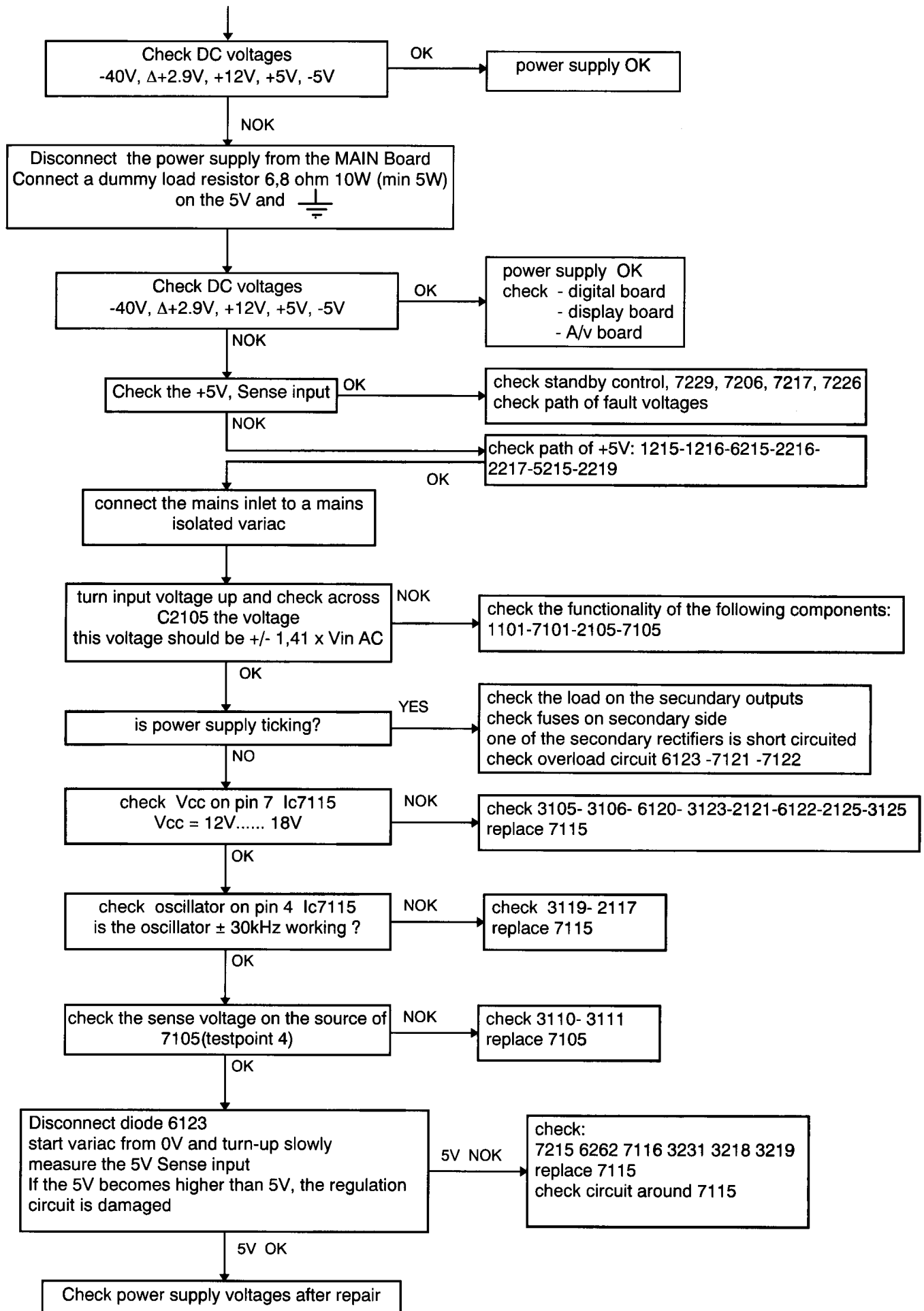
The +12V and -5V have separate voltage regulators(7205, 7225).

The standby control signal coming from the SLAVE processor switches off the +5V, +12V and -5V via transistor 7229 and MOSFETS 7206, 7216, 7226.

+5VSTB is fed to the display board.

-40V is fed to the display board which is resending a voltage VGL-1(-30,7V). After adding +2,9V via regulator 7256, this voltage is fed to the display board(VGL+1).

## TROUBLESHOOTING POWER SUPPLY

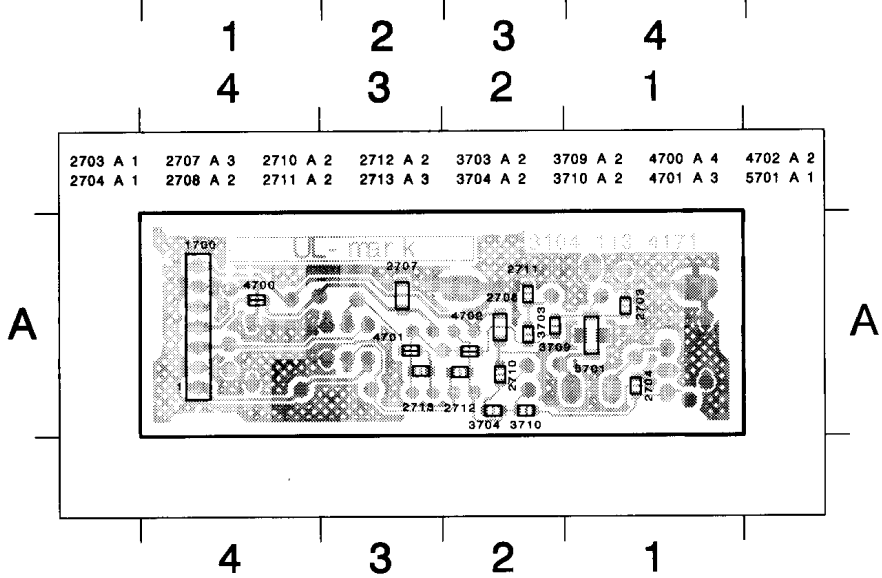
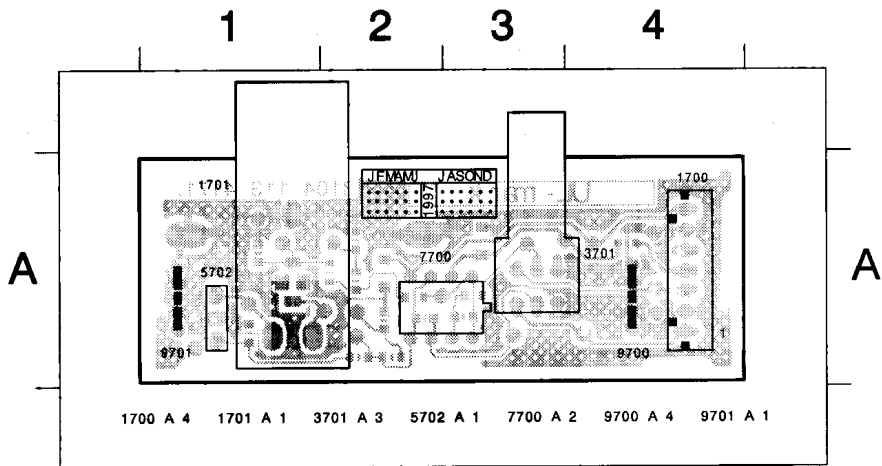
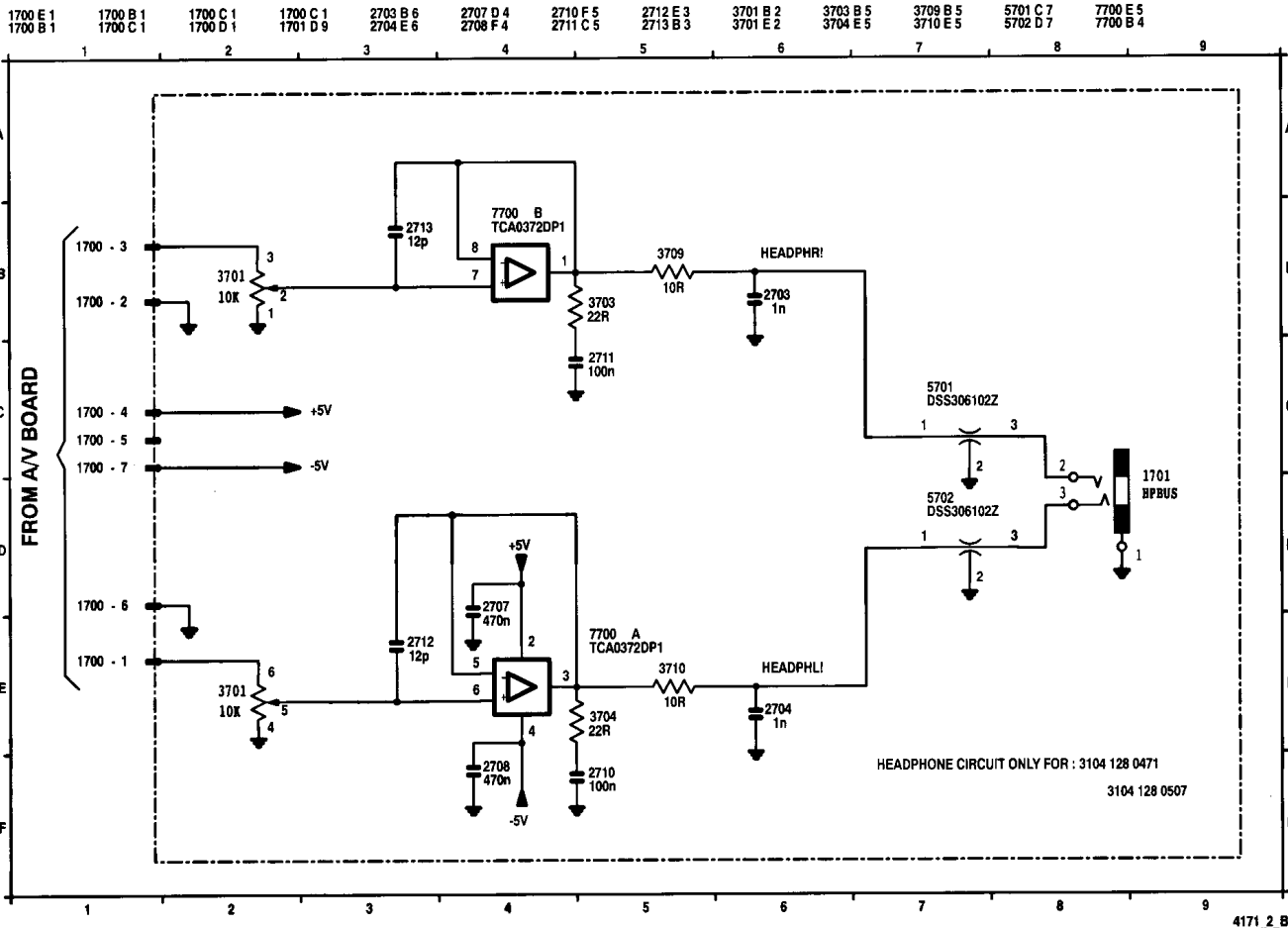




## ELECTRICAL PARTSLIST POWER SUPPLY BOARD

1005	4822 218 11814	POWER SUPPLY UNIT							
<b>MISCELLANEOUS</b>									
0101	▲ 4822 265 31015	MAINS INLET							
1101	▲ 4822 070 31002	FUSE 218001.(1A)							
1215	▲ 4822 252 11144	FUSE 19398E1(3,150A)							
1216	▲ 4822 252 11144	FUSE19398E1(3,150A)							
<b>CAPACITORS</b>									
2101	▲ 4822 121 70677	330nF20%	275V						
2102	▲ 4822 126 12644	100pF20%	400V						
2103	▲ 4822 126 12644	100pF20%	400V						
2105	4822 124 12098	100µF 20%	385V						
2113	▲ 4822 126 13841	1nF 20%	250V						
2115	4822 121 42408	220nF 5%	63V						
2116	4822 124 12099	6,8nF 20%	63V						
2117	4822 121 43179	18nF 5%	250V						
2118	5322 122 32818	2,2nF 10%	100V						
2120	5322 122 32818	2,2nF 10%	100V						
2121	4822 124 40433	47µF20%	25V						
2125	4822 124 40246	4,7µF20%	63V						
2202	4822 124 42382	100µF20%	50V						
2206	5322 124 21189	100µF20%	40V						
2207	5322 124 21189	100µF20%	40V						
2216	4822 124 41335	3300µF20%	10V						
2217	4822 124 41335	3300µF20%	10V						
2218	5322 121 42386	100nF 5%	63V						
2219	4822 124 41335	3300µF20%	10V						
2225	4822 124 12099	6,8nF 20%	63V						
2226	4822 124 40184	1000µF20%	10V						
2227	4822 124 40184	1000µF20%	10V						
2229	5322 122 32818	2,2nF 10%	100V						
2251	4822 124 42382	100µF20%	50V						
2252	4822 050 11003	10K 1%	0,4W						
2256	5322 124 21189	100µF20%	40V						
2257	5322 124 21189	100µF20%	40V						
2260	4822 124 42382	100µF20%	50V						
<b>RESISTORS</b>									
3101	4822 116 30478	20Ω 20%	2W						
3103	▲ 4822 053 20474	470k 5%	0,25W						
3104	4822 053 20474	470k 5%	0,25W						
3105	4822 053 11123	12k 5%	2W						
3106	4822 053 11123	12k 5%	2W						
3107	4822 116 52228	680Ω 5%	0,5W						
3108	4822 116 52189	30Ω 5%	0,5W						
3109	4822 116 83864	10k 5%	0,5W						
3110	4822 116 80176	1Ω 5%	0,5W						
3111	4822 116 80176	1Ω 5%	0,5W						
3115	4822 116 52207	1k2 5%	0,5W						
3116	4822 116 83864	10k 5%	0,5W						
3117	4822 116 83864	10k 5%	0,5W						
3118	4822 116 83864	10k 5%	0,5W						
3119	4822 116 52246	1k6 5%	0,5W						
3121	4822 116 52246	1k6 5%	0,5W						
3122	4822 116 52246	1k6 5%	0,5W						
3123	4822 116 83883	470Ω 5%	0,5W						
3124	4822 116 52207	1k2 5%	0,5W						
3125	▲ 4822 052 10109	10Ω 5%	0,33W						
3201	▲ 4822 052 10228	2Ω20 5%	0,33W						
3216	4822 116 52207	1k2 5%	0,5W						
3217	4822 116 52234	100k 5%	0,5W						
3218	4822 050 12492	2k49 1%	0,4W						
3219	4822 050 12322	2k32 1%	0,4W						
3220	4822 116 52187	24 Ω 5%	0,5W						
3221	4822 116 52175	100Ω 5%	0,5W						
3222	4822 116 52175	100Ω 5%	0,5W						
3223	4822 116 52175	100Ω 5%	0,5W						
3224	4822 116 52175	100Ω 5%	0,5W						
3226	4822 116 83864	10k 5%	0,5W						
3227	4822 116 52297	68k 5%	0,5W						
3229	4822 116 83864	10k 5%	0,5W						
3230	4822 116 83864	10k 5%	0,5W						
3231	▲ 4822 052 10101	100Ω 5%	0,33W						
3239	4822 116 52207	1k2 5%	0,5W						
3251	▲ 4822 116 82438	0Ω22 5%							
3256	▲ 4822 052 10108	1Ω 5%	0,33W						
3257	4822 116 52219	330Ω 5%	0,5W						
3258	4822 116 52216	240Ω 5%	0,5W						
3259	▲ 4822 052 10108	1Ω 5%	0,33W						
3260	5322 116 82222	1Ω2 5%	0,5W						
<b>COILS</b>									
5101	4822 157 53348	FILTER CHOKE ASSY							
CU15D									
5102	▲ 4822 146 10908	SM TRANSFORMER -							
CE26C									
5215	4822 157 11448	6,8µH (R635LY-6R8M)							
<b>DIODES</b>									
6105	4822 130 30621	1N4148							
6115	4822 130 30621	1N4148							
6120	4822 130 34499	BZX79-B20							
6122	4822 130 30621	1N4148							
6123	4822 130 34499	BZX79-B20							
6125	4822 130 42489	BYD33G							
6201	4822 130 42489	BYD33G							
6205	5322 130 31938	BYV27-2							
6215	4822 130 83801	PBYR745F							
6225	4822 130 42489	BYD33G							
6251	4822 130 42489	BYD33G							
6257	4822 130 42489	BYD33G							
6260	4822 130 32245	BYV10-40							
6261	4822 130 32245	BYV10-40							
6262	4822 130 30621	1N4148							
<b>IC's</b>									
7101	4822 130 83707	RECTIFIER S1NB80							
7105	4822 130 63689	STP3N60FI							
7115	4822 209 90755	UC3842AN							
7116	▲ 4822 130 10025	CNX82A							
7121	4822 130 41023	BC328-16							
7122	4822 130 40892	BC338-16							
7205	4822 209 81726	MC7812CT							
7206	5322 209 70394	BUK455-50A							
7215	4822 209 81397	TL431CLPST							
7216	5322 209 70394	BUK455-50A							
7217	4822 130 41937	BS170							
7225	4822 209 72684	L7905CV							
7226	5322 209 70394	BUK455-50A							
7229	4822 130 40892	BC338-16							
7256	4822 209 80591	LM317T							

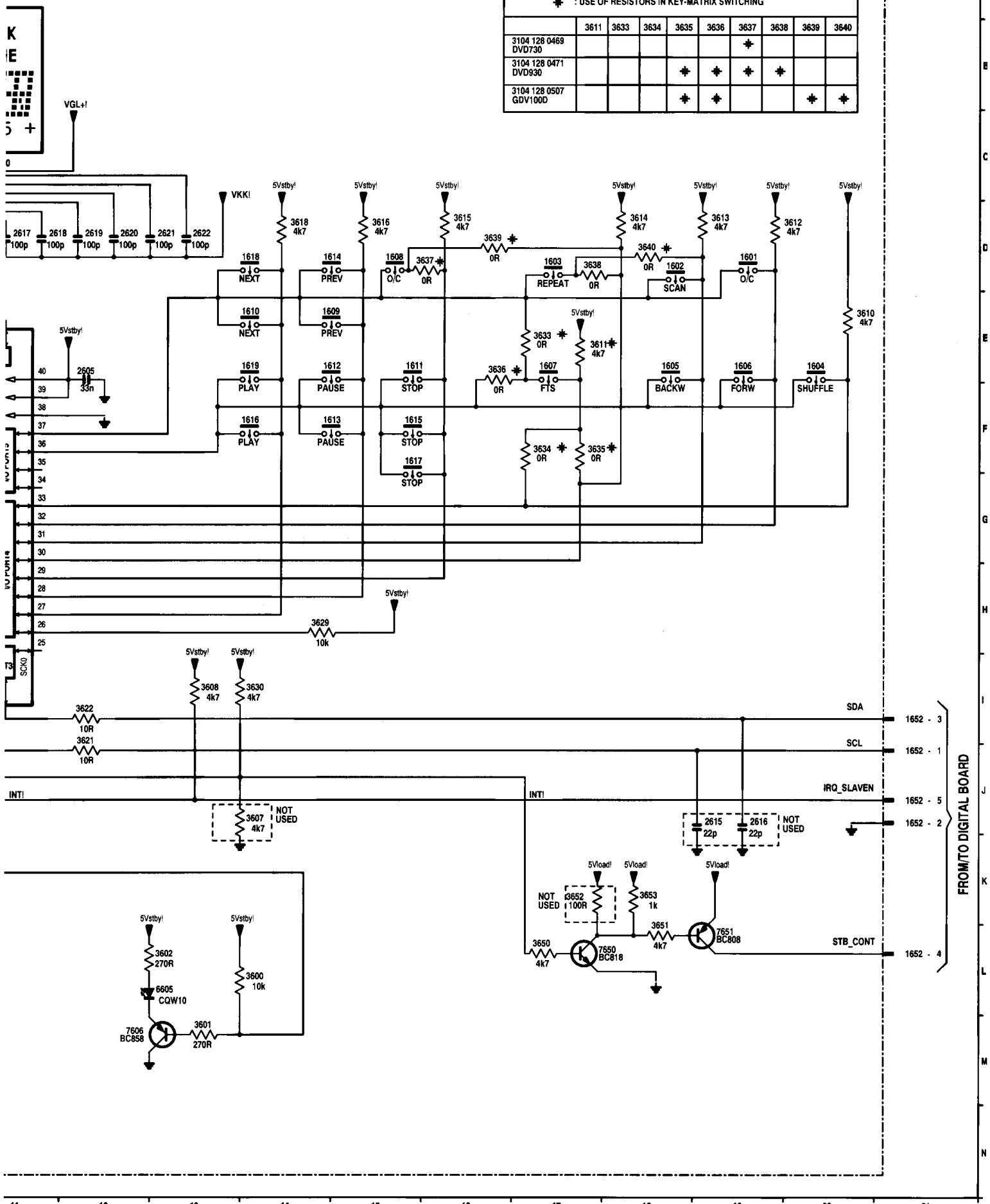
HEADPHONE





3601 M13	3605 J10	3609 M7	3613 D19	3618 D14	3622 I12	3626 J7	3633 E17	3637 D16	3650 L17	6605 L13	6610 L10	7607 H3
3602 L13	3606 J9	3610 E20	3614 D18	3619 J8	3623 J7	3629 H14	3634 F17	3638 D17	3651 L18	6606 H3	7600 E6	7650 L17
3603 G2	3607 J14	3611 E17	3615 D16	3620 L8	3624 J7	3630 I14	3635 F17	3639 D16	3652 K17	6607 G4	7604 L8	7651 L19
3604 G5	3608 I13	3612 D20	3616 D15	3621 I12	3625 J7	3631 L7	3636 E16	3640 D18	3653 K18	6609 M6	7606 M12	

11 12 13 14 15 16 17 18 19 20 21

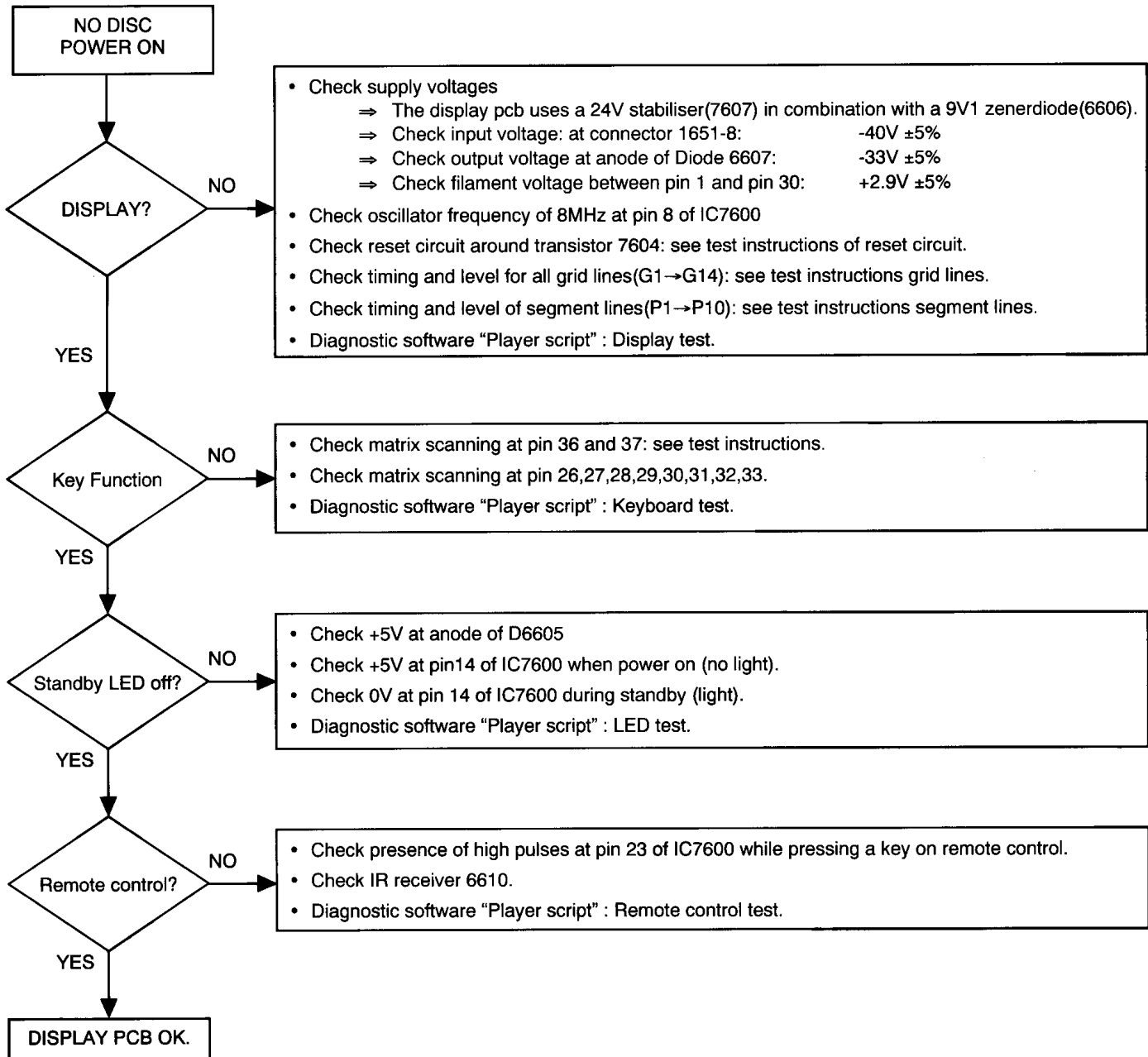


\* : USE OF RESISTORS IN KEY-MATRIX SWITCHING

	3611	3633	3634	3635	3636	3637	3638	3639	3640
3104 128 0469 DVD730						*			
3104 128 0471 DVD930				*	*	*	*		
3104 128 0507 GDV100D				*	*			*	*

FROM/DIGITAL BOARD

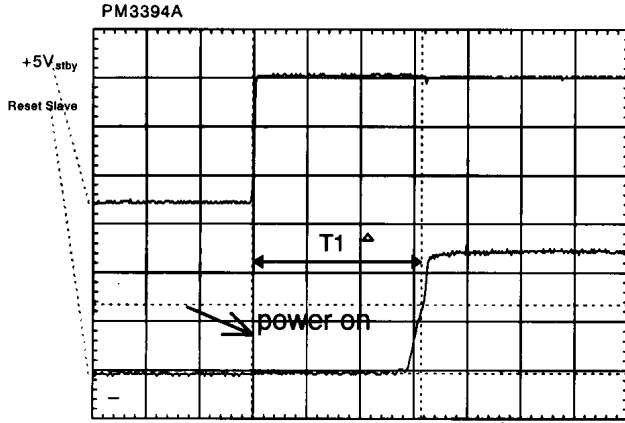
### TROUBLESHOOTING DISPLAY BOARD



## TEST INSTRUCTIONS

### Test of reset circuit:

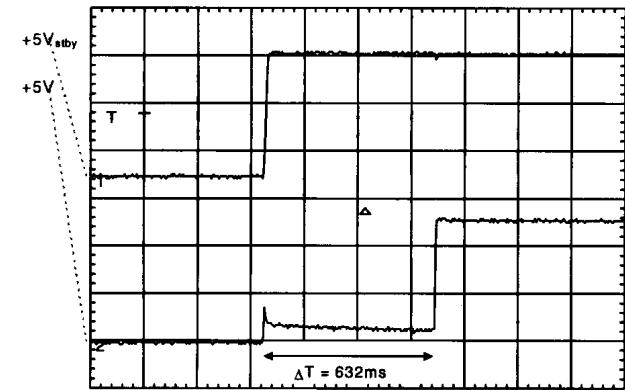
Check next reset timing with an oscilloscope at pin 10 of  $\mu$ processor.7600:



Timing: 400msec < T1 < 700msec.

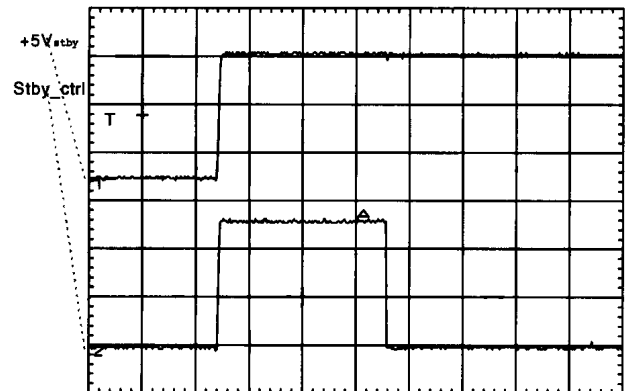
### +5V after +5Vstby

+5V to be measured on power supply connector 0201-1+2



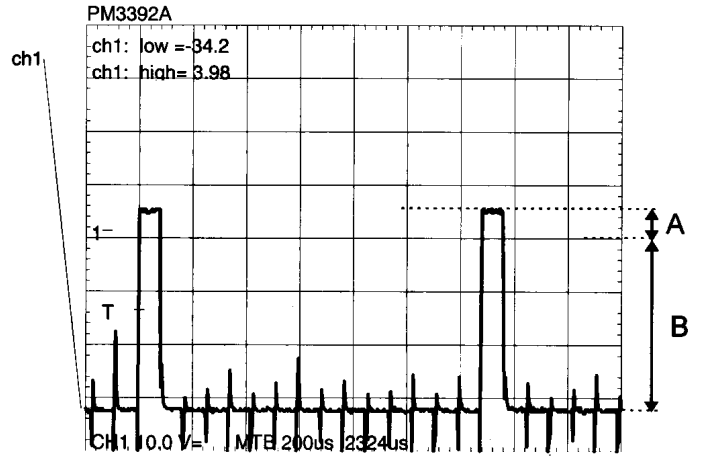
### Standby control after power-up in relation to +5Vstby

Stby\_ctrl to be measured on connector 1652-4.



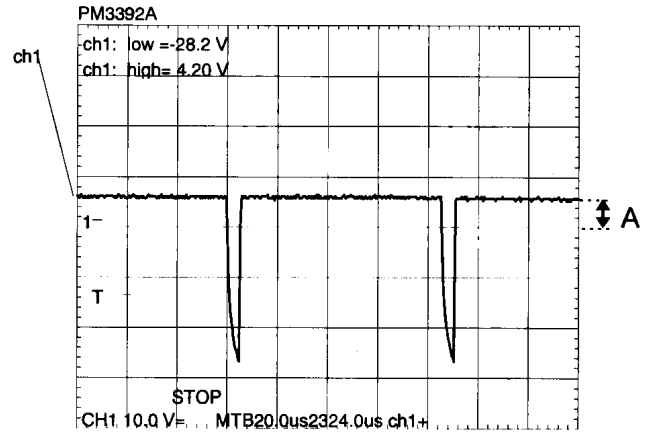
### Test of grid lines:

Check next timing and level for all grid lines (G1 → G14).



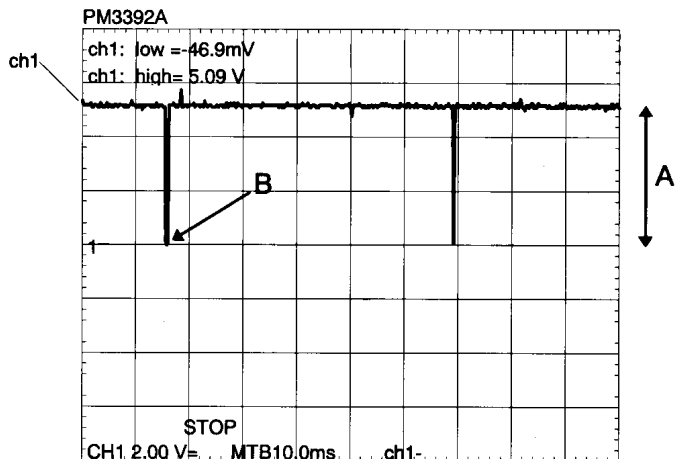
### Test of segment lines

Check timing and levels of segment lines P1 → P10:



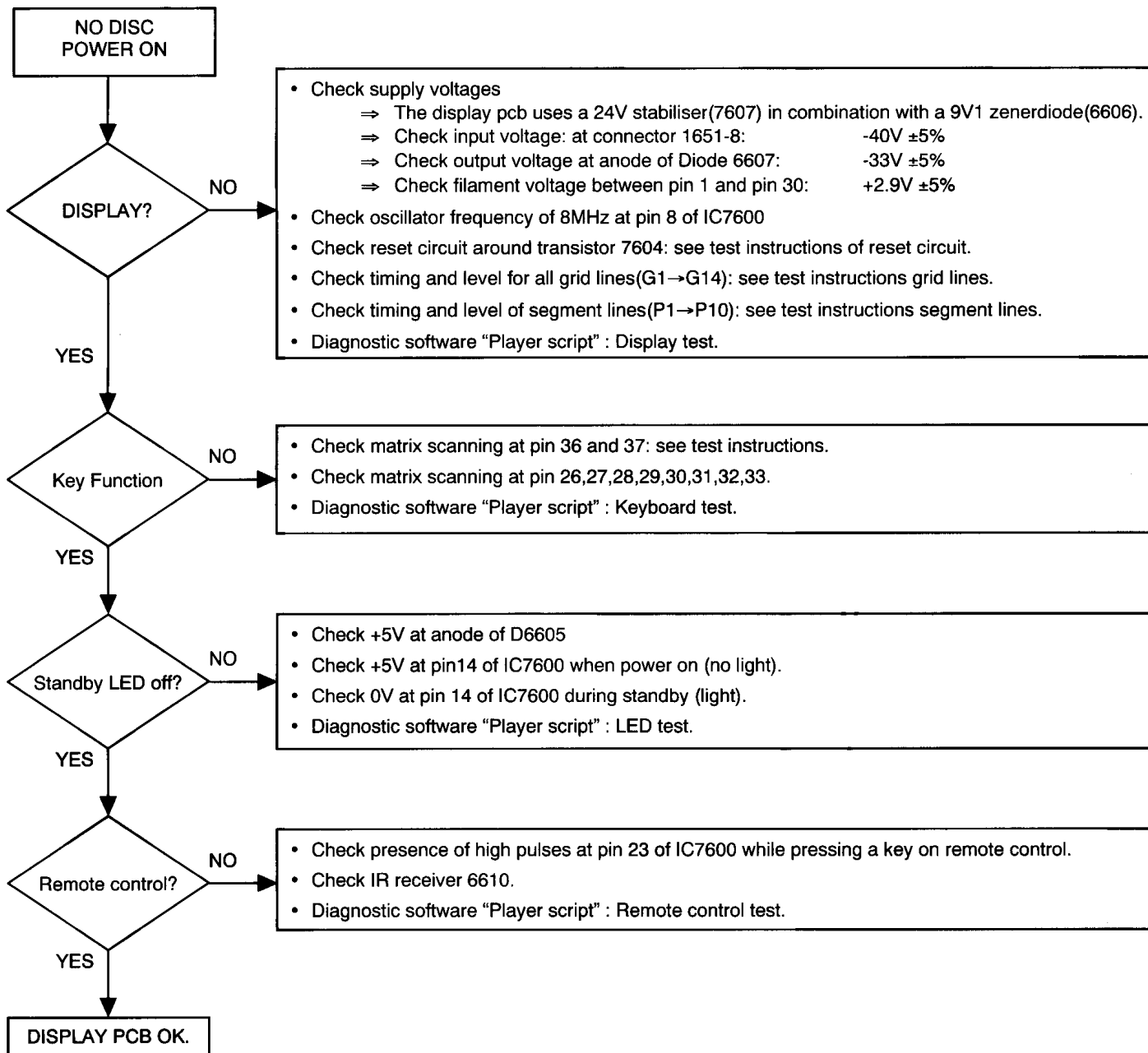
### Test of Key-matrix:

Connect a extra 10kΩ pull-up to pin 36 en 37 of the  $\mu$ P and check next matrix scanning at these pins.



Check matrix scanning from pin 26 until 33 of the  $\mu$ P. The results should be the same as the diagram above.

## TROUBLESHOOTING DISPLAY BOARD



## TMP87C874F : SLAVE microprocessor(IC7600)

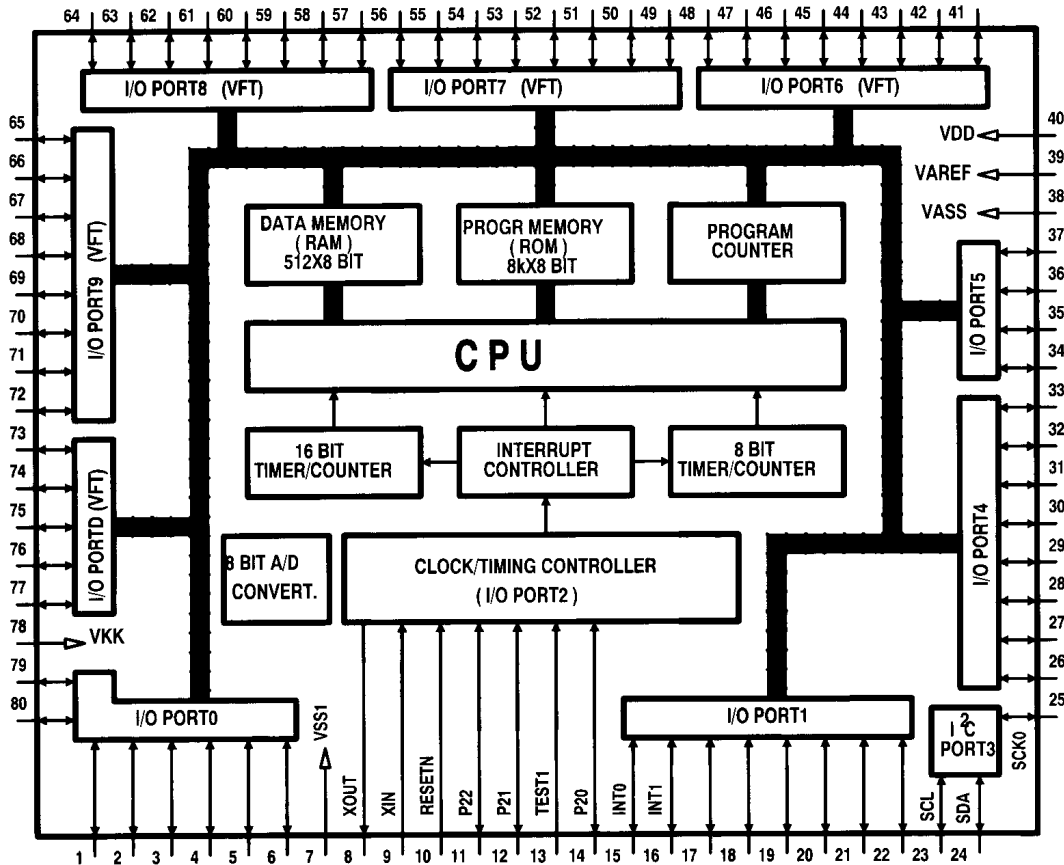
### Description

TMP87C874F is a high speed and high performance 8-bit single chip microcomputer, containing 8-bit A/D conversion inputs and a VFT(Vacuum Fluorescent Tube) driver.

In this application, it is used as SLAVE microprocessor and as VFTD driver. All the communication to the digital board runs via the Serial bus interface(I2C).

### Block diagram

TMP87C874F



### Pin descriptions

INT0	external interrupt input 0
INT1	external interrupt input 1
RESETN	reset signal input, active low
SCL	I2C-bus serial clock input/output
SDA	I2C-bus serial data input/output
TEST	test pin, tied to low
VAREF	analog reference voltage input
VASS	analog reference ground
VDD	+5V
VKK	VFT driver power supply
VSS	ground
XIN, XOUT	resonator connecting pins for high-frequency clock



## ELECTRICAL PARTSLIST HEADPHONE &amp; DISPLAY BOARD

## DISPLAY BOARD

## MISCELLANEOUS

1600	4822 256 92151	DISPLAY HOLDER
1601	4822 135 00156	DISPLAY 14-ST-18GK
1601	4822 276 13114	TACT SWITCH
1619	4822 276 13114	TACT SWITCH
1621	4822 242 10753	CRYSTAL 8 MHz

## CAPACITORS

2600	4822 122 33496	100nF 10%X7R 63V
2601	4822 122 33064	330nF80%Y5V 25V
2602	5322 122 34123	1nF 10%X7R 50V
2603	4822 122 33342	33nF 10%X7R 63V
2604	5322 122 32654	22nF 10%X7R 63V
2605	4822 122 33342	33nF 10%X7R 63V
2606	5322 122 32658	22pF 5% 50V
2607	5322 122 32658	22pF 5% 50V
2608	5322 122 32654	22nF 10%X7R 63V
2609	4822 124 22649	10µF 20% 16V
2617	5322 122 32531	100pF 5%NP 50V
2618	5322 122 32531	100pF 5%NP 50V
2619	5322 122 32531	100pF 5%NP 50V
2620	5322 122 32531	100pF 5%NP 50V
2621	5322 122 32531	100pF 5%NP 50V
2622	5322 122 32531	100pF 5%NP 50V
2623	4822 124 80483	47µF20% 6,3V

## RESISTORS

3600	4822 117 10833	10k 1% 0,1W
3601	4822 051 20271	270Ω 5% 0,1W
3602	4822 051 20271	270Ω 5% 0,1W
3603 ▲	4822 117 11152	4Ω7 5%
3604	4822 117 10834	47k 1% 0,1W
3605	4822 051 20008	0Ω JUMP. (0805)
3606	4822 051 20008	0Ω JUMP. (0805)
3608	4822 051 20472	4k7 5% 0,1W
3609	4822 051 20104	100k 5% 0,1W
3610	4822 051 20472	4k7 5% 0,1W
3612	4822 051 20472	4k7 5% 0,1W
3613	4822 051 20472	4k7 5% 0,1W
3614	4822 051 20472	4k7 5% 0,1W
3615	4822 051 20472	4k7 5% 0,1W
3616	4822 051 20472	4k7 5% 0,1W
3618	4822 051 20472	4k7 5% 0,1W
3620	4822 051 10102	1k 2% 0,25W
3621	4822 051 20109	10Ω 5% 0,1W
3622	4822 051 20109	10Ω 5% 0,1W
3629	4822 117 10833	10k 1% 0,1W
3630	4822 051 20472	4k7 5% 0,1W
3631	4822 117 10833	10k 1% 0,1W
3637	4822 051 20008	0Ω JUMP. (0805)
3650	4822 051 20472	4k7 5% 0,1W
3651	4822 051 20472	4k7 5% 0,1W
3653	4822 050 21002	1k 1% 0,6W
4600	4822 051 10008	0Ω 5% 0,25W
4602	4822 051 10008	0Ω 5% 0,25W
4603	4822 051 10008	0Ω 5% 0,25W
4604	4822 051 10008	0Ω 5% 0,25W
4605	4822 051 10008	0Ω 5% 0,25W
4606	4822 051 10008	0Ω 5% 0,25W
4607	4822 051 20008	0Ω JUMP. (0805)
4608	4822 051 10008	0Ω 5% 0,25W

4609	4822 051 10008	0Ω 5% 0,25W
4610	4822 051 10008	0Ω 5% 0,25W
4614	4822 051 10008	0Ω 5% 0,25W
4615	4822 051 10008	0Ω 5% 0,25W
4616	4822 051 20008	0Ω JUMP. (0805)
4617	4822 051 20008	0Ω JUMP. (0805)
4618	4822 051 10008	0Ω 5% 0,25W
4619	4822 051 10008	0Ω 5% 0,25W
4620	4822 051 10008	0Ω 5% 0,25W
4621	4822 051 10008	0Ω 5% 0,25W
4622	4822 051 10008	0Ω 5% 0,25W
4623	4822 051 20008	0Ω JUMP. (0805)
4624	4822 051 10008	0Ω 5% 0,25W
4625	4822 051 20008	0Ω JUMP. (0805)

## DIODES

6605	4822 130 11089	TLHR4400-SC36-AMMO
6606	4822 130 11047	BZX284-C9V1
6607	4822 130 11088	BZX284-C2V4
6609	4822 130 83757	BAS216
6610	4822 130 10165	GP1U28XP

## TRANSISTORS

7600	4822 209 16055	TMP87PM74ZF
7604	5322 130 42136	BC848C
7606	4822 130 42513	BC858C
7607	4822 209 31257	MC79L24ACP
7650	4822 130 42616	BC818-40
7651	4822 130 42655	BC808-40

## HEADPHONE BOARD

1701	4822 267 31453	HEADPHONE SOCKET
2703	5322 122 34123	1nF10%X7R 50V
2704	5322 122 34123	1nF10%X7R 50V
2707	4822 124 12096	470nF 10% X7R 16V
2708	4822 124 12096	470nF 10% X7R 16V
2710	4822 126 14165	100nF 10% 25V
2711	4822 126 14165	100nF 10% 25V
2712	4822 122 32139	12pF 2%NP0 63V
2713	4822 122 32139	12pF 2%NP0 63V
3701	4822 101 21199	10kX2 20% 0,025W
3703	4822 051 20229	22 Ω 5% 0,1W
3704	4822 051 20229	22 Ω 5% 0,1W
3709	4822 051 20109	10 Ω 5% 0,1W
3710	4822 051 20109	10 Ω 5% 0,1W
5701	4822 242 10805	1000pF
5702	4822 157 11402	100V 1n 20%
7700	4822 209 62059	TCA0372DP1

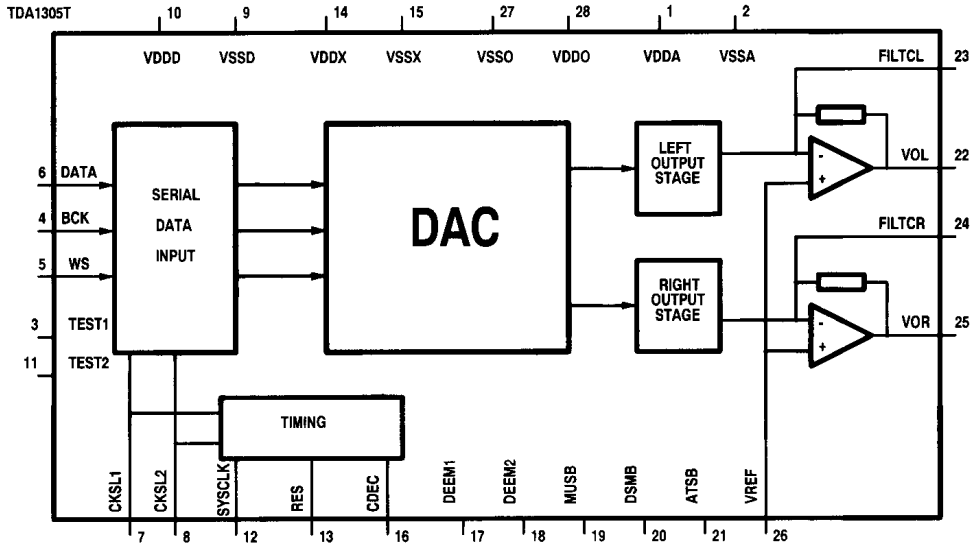
## TDA1305T : Bitstream continuous calibration DAC(IC7503)

### General description

The TDA1305T is a dual CMOS DAC with upsampling filter and noise shaper. The combination of high oversampling up to 16FS, 2nd order noise shaping and continuous calibration conversion ensures that only simple 1st order analog post-filtering is required.

Two on board operational amplifiers convert the digital-to-analog current to an output voltage. Externally connected capacitors perform the required 1st order filtering so that no further post-filtering is required.

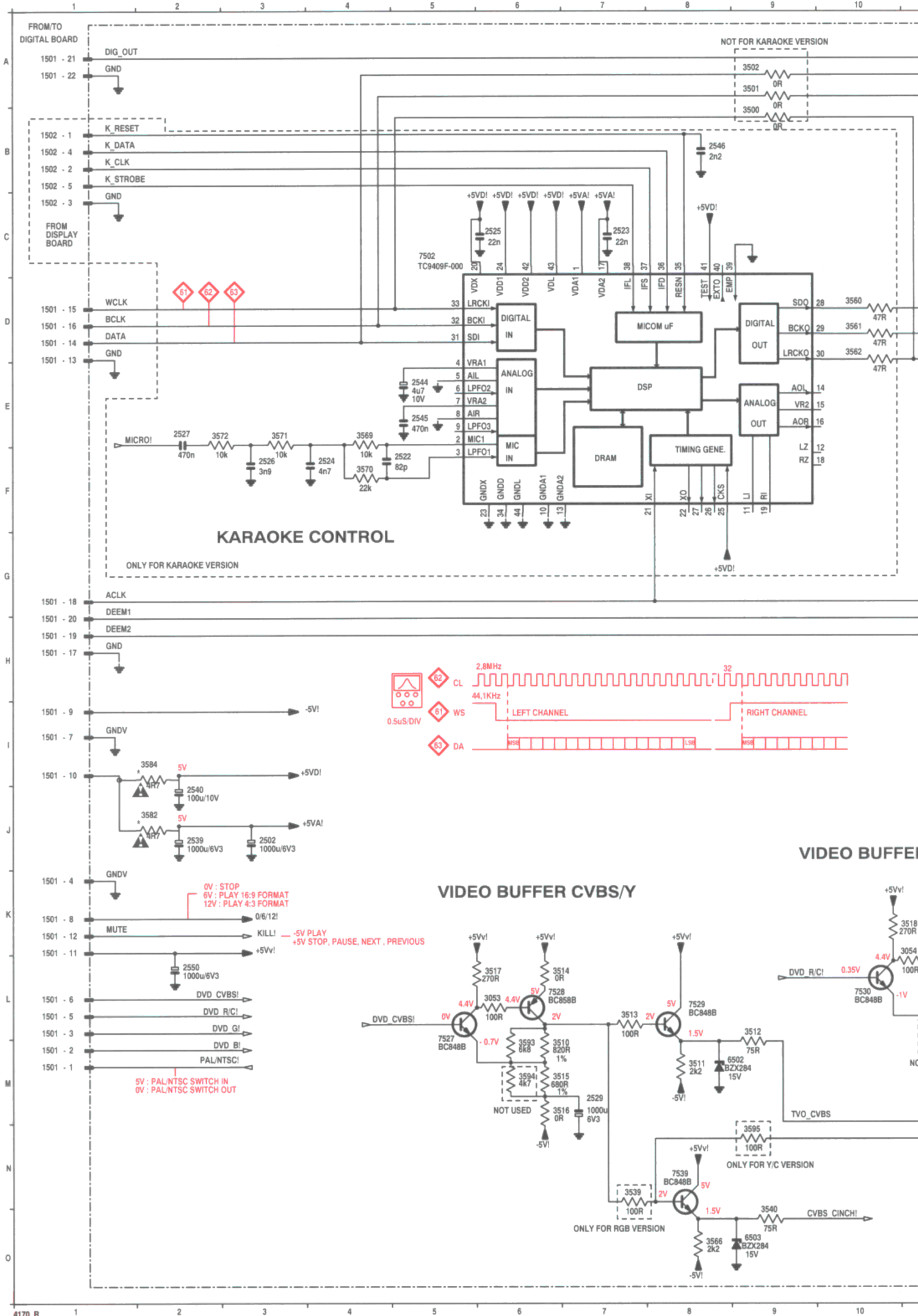
### Block diagram

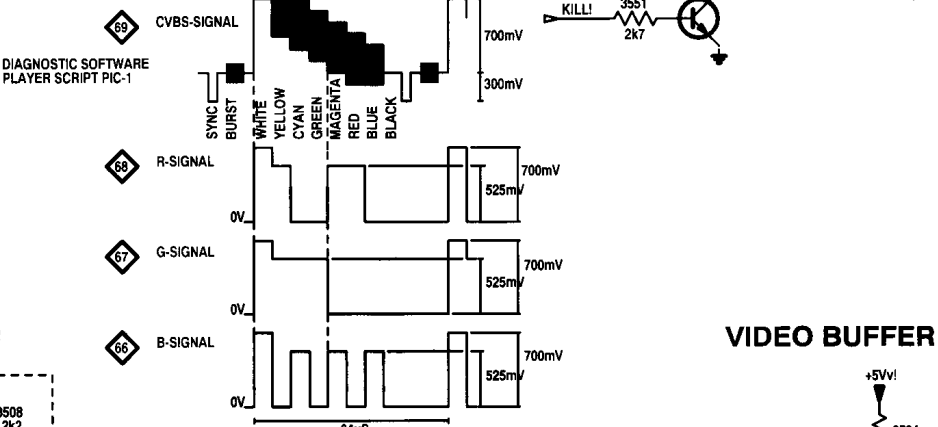
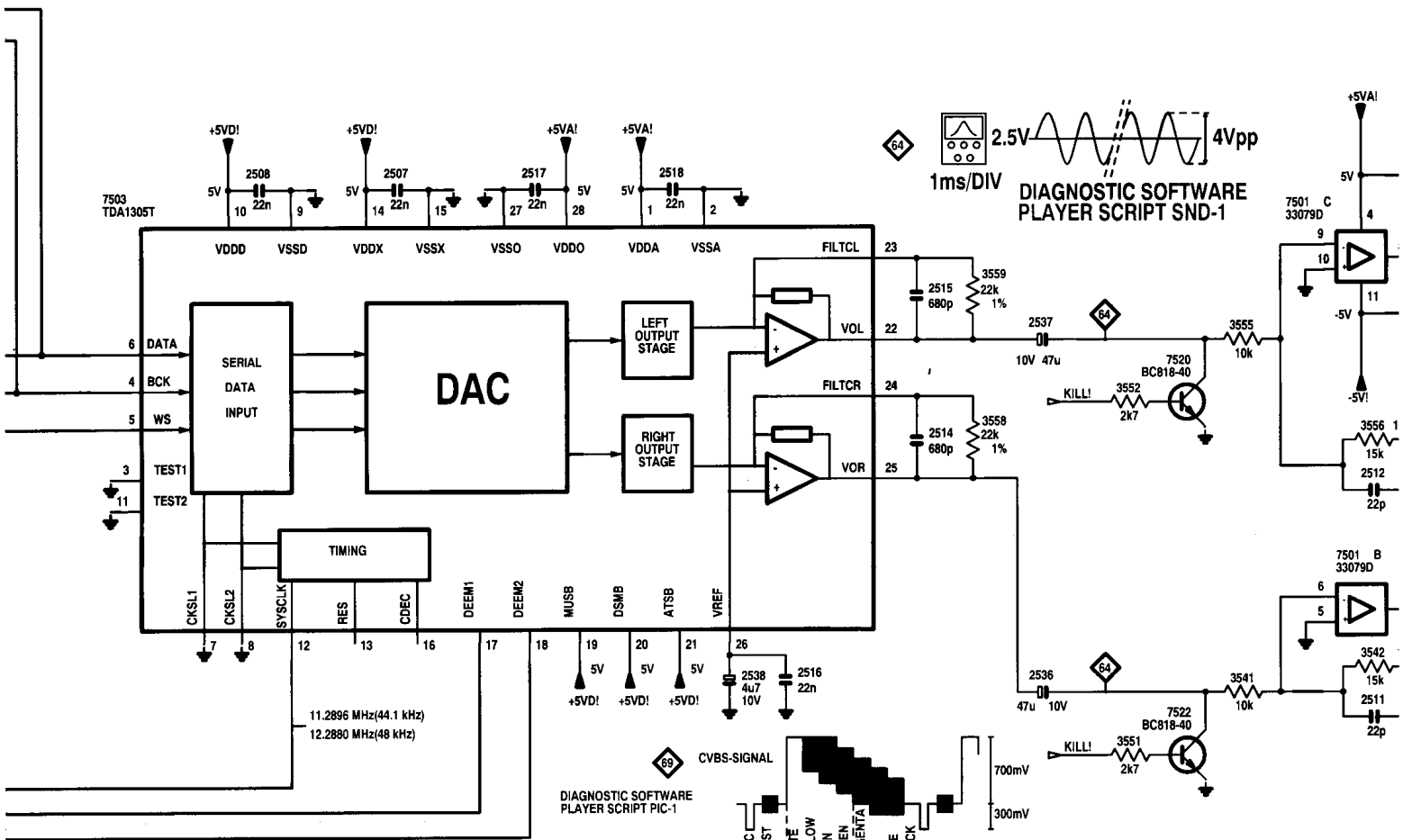


### Pin description

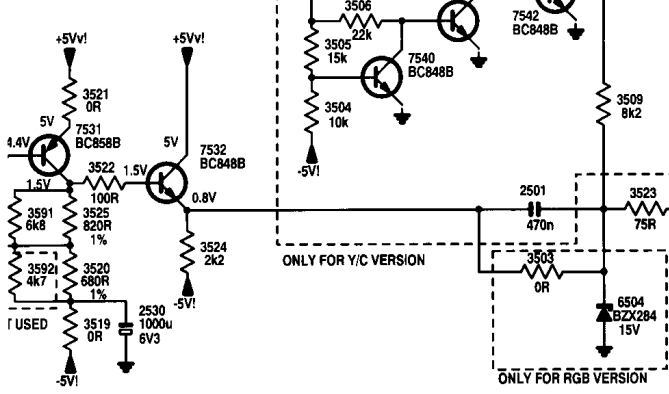
PIN	NAME	I/O	DESCRIPTION
1	VDDA	-	Positive supply voltage(analog part)
2	VSSA	-	supply ground(analog part)
3	TEST1	I	test input(connected to ground)
4	BCK	I	bit clock input
5	WS	I	word select input
6	DATA	I	data input
7	CKSL1	I	clock selection 1
8	CKSL2	I	clock selection 2
9	VSSD	-	supply ground (digital part)
10	VDDD	-	Positive supply voltage (digital part)
11	TEST2	I	test input (connected to ground)
12	SYSCLK	I	system clock
13	RES	-	not connected
14	VDDX	-	Positive supply voltage
15	VSSX	-	supply ground
16	CDEC	O	system clock output
17	DEEM1	I	deemphasis on/off
18	DEEM2	I	deemphasis on/off
19	MUSB	I	muting (active low)
20	DSMB	I	double speed mode
21	ATSB	I	12 dB attenuation
22	VOL	O	left channel output
23	FILTCL	I	capacitor for left channel 1st order filter
24	FILTCR	I	capacitor for right channel 1st order filter
25	VOR	O	right channel output
26	VREF	O	internal reference voltage for output channels (VDD/2)
27	VSSO	-	supply ground (operational amplifier)
28	VDDO	-	positive supply voltage (operational amplifier)

AUDIO/VIDEO SCART CIRCUIT DIAGRAM

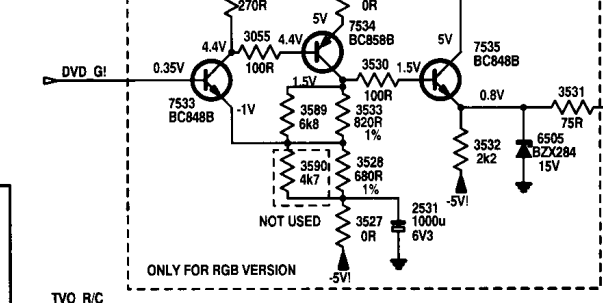




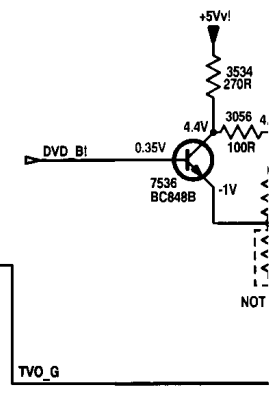
### RED/CHROMA



### VIDEO BUFFER GREEN

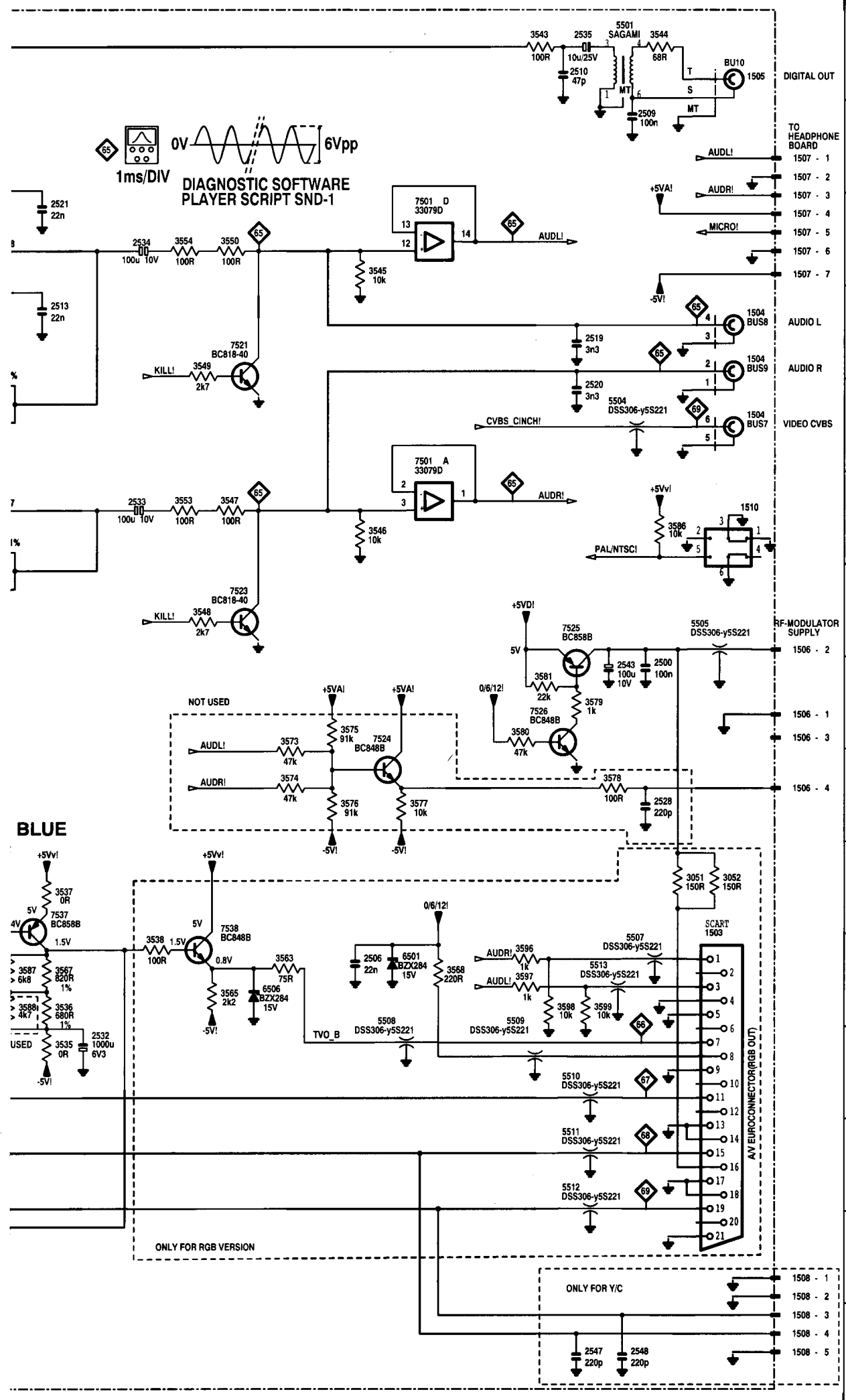


### VIDEO BUFFER



VERSIONS	
3104 128 0466	RGB/SCART VERSION
3104 128 0467	Y/C VERSION
3104 128 0468	Y/C + KARAOKE VERSION

22 23 24 25 26 27 28 29 30



1501	M 1	3563	K25
1501	M 1	3565	K24
1501	L 1	3566	O 8
1501	K 1	3567	K22
1501	L 1	3568	K27
1501	L 1	3569	E 4
1501	L 1	3570	F 4
1501	K 1	3571	C 3
1501	L 1	3572	E 2
1501	L 1	3573	H25
1501	L 1	3574	I25
1501	K 1	3575	H25
1501	E 1	3576	I25
1501	D 1	3577	I26
1501	D 1	3578	I28
1501	D 1	3579	H28
1501	H 1	3580	H27
1501	G 1	3581	H28
1501	H 1	3582	J 2
1501	H 1	3584	I 2
1501	A 1	3586	F29
1501	A 1	3587	K22
1502	B 1	3588	K22
1502	B 1	3589	K18
1502	C 1	3590	L18
1502	B 1	3591	L11
1502	B 1	3592	L11
1503	K29	3593	M 6
1504	D30	3594	M 6
1504	D30	3595	N 9
1504	E30	3596	K28
1505	A30	3597	K28
1506	H30	3598	K28
1506	H30	3599	K28
1506	H30	3600	A29
1506	I30	3601	E28
1507	B30	3602	G29
1507	B30	3603	K29
1507	C30	3604	K26
1507	C30	3605	K27
1507	C30	3606	L28
1507	C30	3607	M28
1507	C30	3608	M28
1508	N30	3609	K28
1508	N30	3610	K28
1508	O30	3611	M 9
1508	O30	3612	O 9
1508	O30	3613	M15
1510	F30	3614	F30
1510	F30	3615	H29
1510	F30	3616	H29
1510	F30	3617	H29
1510	F30	3618	H29
1510	F30	3619	H29
1510	F30	3620	H29
1510	F30	3621	H29
1510	F30	3622	H29
1510	F30	3623	H29
1510	F30	3624	H29
1510	F30	3625	H29
1510	F30	3626	H29
1510	F30	3627	H29
1510	F30	3628	H29
1510	F30	3629	H29
1510	F30	3630	H29
1510	F30	3631	H29
1510	F30	3632	H29
1510	F30	3633	H29
1510	F30	3634	H29
1510	F30	3635	H29
1510	F30	3636	H29
1510	F30	3637	H29
1510	F30	3638	H29
1510	F30	3639	H29
1510	F30	3640	H29
1510	F30	3641	H29
1510	F30	3642	H29
1510	F30	3643	H29
1510	F30	3644	H29
1510	F30	3645	H29
1510	F30	3646	H29
1510	F30	3647	H29
1510	F30	3648	H29
1510	F30	3649	H29
1510	F30	3650	H29
1510	F30	3651	H29
1510	F30	3652	H29
1510	F30	3653	H29
1510	F30	3654	H29
1510	F30	3655	H29
1510	F30	3656	H29
1510	F30	3657	H29
1510	F30	3658	H29
1510	F30	3659	H29
1510	F30	3660	H29
1510	F30	3661	H29
1510	F30	3662	H29

22 23 24 25 26 27 28 29 30



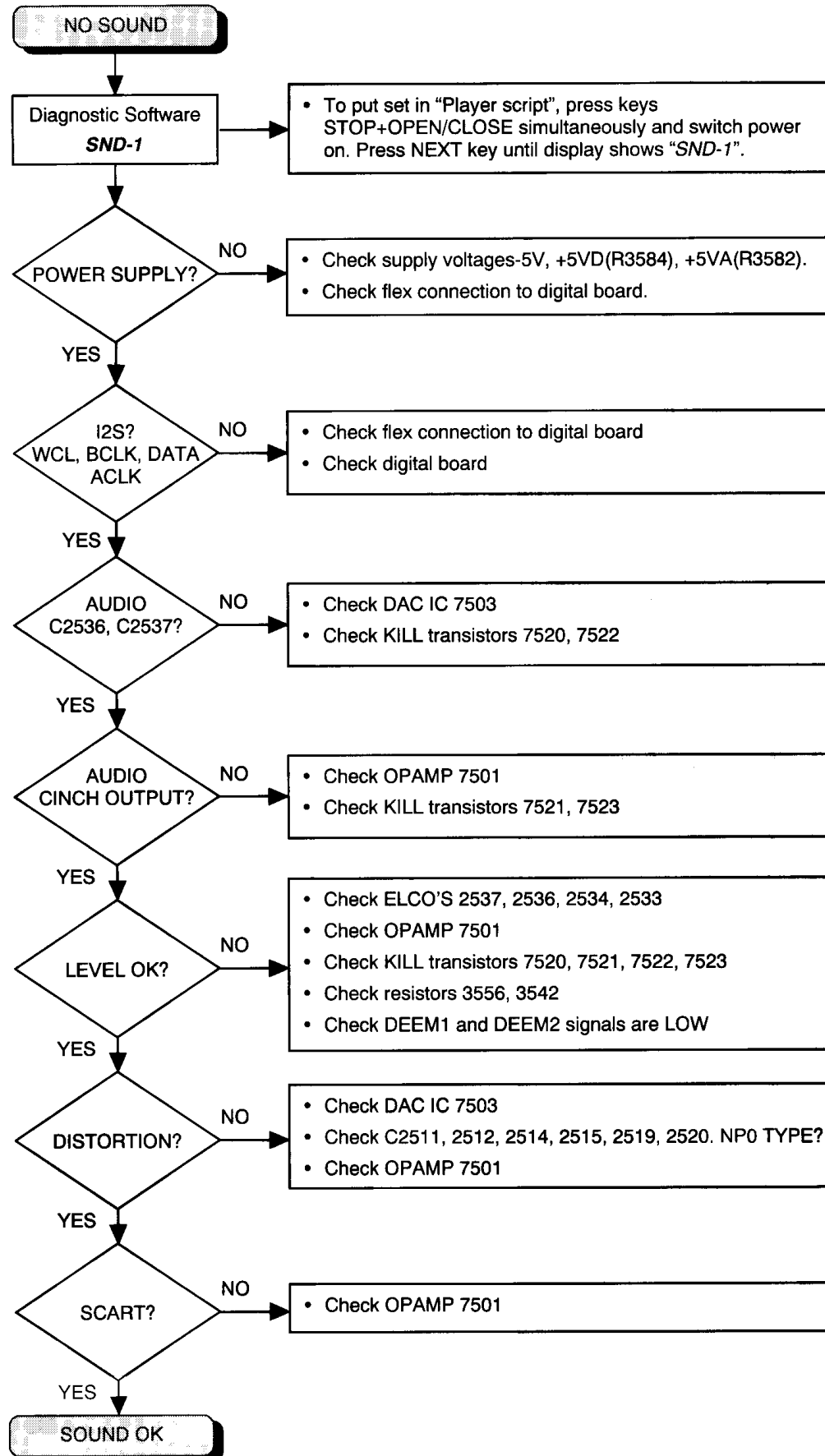
## TROUBLESHOOTING A/V MUX BOARD

Testing of A/V MUX board can be done using diagnostic software "Player script".

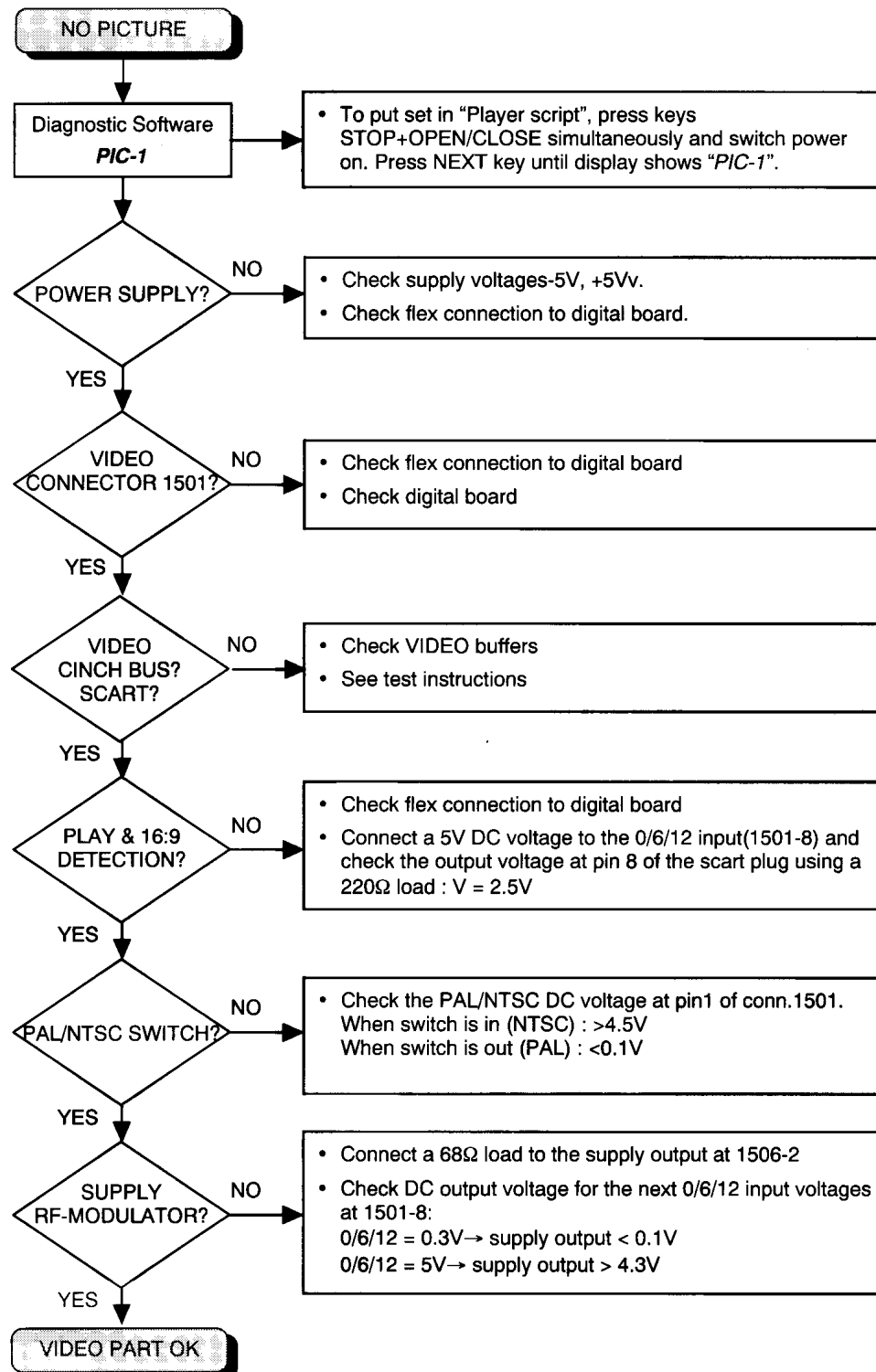
Use digital board to generate a sinus with the first soundtest SND-1 and to generate a CVBS signal with the first picture test PIC-1. See description in chapter "Diagnostic Software : Script Interfaces"

REMARK : Although the "Dealer Script" may result in "Pass", it is possible that the set doesn't output sound or picture because the A/V MUX board hasn't been tested during this test.

### AUDIO PART



**VIDEO PART**





## ELECTRICAL PARTSLIST A/V-MUX BOARD

## MISCELLANEOUS

1501	4822 265 11154	FLEX CONNECTOR 22P
1503	4822 265 11155	SCART SOCKET (21P F.)
1505	4822 267 31729	CON BM CINCH H 1P F
1510	4822 276 13387	SWITCH NTSC/PAL

## CAPACITORS

2500	4822 122 33496	100nF 10%X7R 63V
2502	4822 124 80622	470μF 35V
2506	5322 122 32654	22nF 10%X7R 63V
2507	5322 122 32654	22nF 10%X7R 63V
2508	5322 122 32654	22nF 10%X7R 63V
2509	4822 122 33496	100nF 10%X7R 63V
2510	5322 122 32452	47pF 5%NP0 63V
2511	5322 122 32658	22pF 5% 50V
2512	5322 122 32658	22pF 5% 50V
2513	5322 122 32654	22nF 10%X7R 63V
2514	5322 126 10184	680pF 5% NPO 50V.
2515	5322 126 10184	680pF 5% NPO 50V.
2516	5322 122 32654	22nF 10%X7R 63V
2517	5322 122 32654	22nF 10%X7R 63V
2518	5322 122 32654	22nF 10%X7R 63V
	4822 123 14041	3,3nF 5% NP0 50V
2520	4822 123 14041	3,3nF 5% NP0 50V
2521	5322 122 32654	22nF 10%X7R 63V
2529	4822 124 80622	470μF 35V
2530	4822 124 80622	470μF 35V
2531	4822 124 80622	470μF 35V
2532	4822 124 80622	470μF 35V
2533	4822 124 22339	100μF 16V
2534	4822 124 22339	100μF 16V
2535	4822 124 41579	10μF 20% 50V
2536	4822 124 41527	47μF 25V
2537	4822 124 41527	47μF 25V
2538	4822 124 40246	4,7μF20% 63V
2539	4822 124 80622	470μF 35V
2540	4822 124 41584	100μF 20% 10V
2543	4822 124 41584	100μF 20% 10V
2550	4822 124 80622	470μF 35V

## RESISTORS

3051	4822 117 10353	150Ω 1% 0,1W
3052	4822 117 10353	150Ω 1% 0,1W
3053	4822 051 20101	100Ω 5% 0,1W
3054	4822 051 20101	100Ω 5% 0,1W
3055	4822 051 20101	100Ω 5% 0,1W
3056	4822 051 20101	100Ω 5% 0,1W
3500	4822 051 20008	0Ω JUMP. (0805)
3501	4822 051 20008	0Ω JUMP. (0805)
3502	4822 051 20008	0Ω JUMP. (0805)
3503	4822 051 20008	0Ω JUMP. (0805)
3510	4822 117 11454	820Ω 1% 0,1W
3511	4822 117 11449	2k2 1% 0,1W
3512	4822 051 20759	75Ω 5% 0,1W
3513	4822 051 20101	100Ω 5% 0,1W
3514	4822 051 20008	0Ω JUMP. (0805)
3515	4822 117 10361	680Ω 1% 0,1W
3516	4822 051 20008	0Ω JUMP. (0805)
3517	4822 051 20271	270Ω 5% 0,1W
3518	4822 051 20271	270Ω 5% 0,1W
3519	4822 051 20008	0Ω JUMP. (0805)
3520	4822 117 10361	680Ω 1% 0,1W
3521	4822 051 20008	0Ω JUMP. (0805)
3522	4822 051 20101	100Ω 5% 0,1W
3523	4822 051 20759	75Ω 5% 0,1W
3524	4822 117 11449	2k2 1% 0,1W

3525	4822 117 11454	820Ω 1% 0,1W
3526	4822 051 20271	270Ω 5% 0,1W
3527	4822 051 20008	0Ω JUMP. (0805)
3528	4822 117 10361	680Ω 1% 0,1W
3529	4822 051 20008	0Ω JUMP. (0805)
3530	4822 051 20101	100Ω 5% 0,1W
3531	4822 051 20759	75Ω 5% 0,1W
3532	4822 117 11449	2k2 1% 0,1W
3533	4822 117 11454	820Ω 1% 0,1W
3534	4822 051 20271	270Ω 5% 0,1W
3535	4822 051 20008	0Ω JUMP. (0805)
3536	4822 117 10361	680Ω 1% 0,1W
3537	4822 051 20008	0Ω JUMP. (0805)
3538	4822 051 20101	100Ω 5% 0,1W
3539	4822 051 20101	100Ω 5% 0,1W
3540	4822 051 20759	75Ω 5% 0,1W
3541	4822 117 10833	10k 1% 0,1W
3542	4822 116 83933	15k 1% 0,1W
3543	4822 051 20101	100Ω 5% 0,1W
3544	4822 051 20689	68Ω 5% 0,1W
3545	4822 117 10833	10k 1% 0,1W
3546	4822 117 10833	10k 1% 0,1W
3547	4822 051 20101	100Ω 5% 0,1W
3548	4822 051 20272	2k70 5% 0,1W
3549	4822 051 20272	2k70 5% 0,1W
3550	4822 051 20101	100Ω 5% 0,1W
3551	4822 051 20272	2k70 5% 0,1W
3552	4822 051 20272	2k70 5% 0,1W
3553	4822 051 20101	100Ω 5% 0,1W
3554	4822 051 20101	100Ω 5% 0,1W
3555	4822 117 10833	10k 1% 0,1W
3556	4822 116 83933	15k 1% 0,1W
3558	4822 117 10354	22k 1% 0,1W
3559	4822 117 10354	22k 1% 0,1W
3563	4822 051 20759	75Ω 5% 0,1W
3565	4822 117 11449	2k2 1% 0,1W
3566	4822 117 11449	2k2 1% 0,1W
3567	4822 117 11454	820Ω 1% 0,1W
3568	4822 117 11503	220Ω 1% 0,1W
3579	4822 051 10102	1k 2% 0,25W
3580	4822 117 10834	47k 1% 0,1W
3581	4822 051 20223	22k 5% 0,1W
3582 ▲	4822 117 11152	4Ω7 5%
3584 ▲	4822 117 11152	4Ω7 5%
3586	4822 117 10833	10k 1% 0,1W
3587	4822 051 20682	6k80 5% 0,1W
3589	4822 051 20682	6k80 5% 0,1W
3591	4822 051 20682	6k80 5% 0,1W
3593	4822 051 20682	6k80 5% 0,1W
3596	4822 051 10102	1k 2% 0,25W
3597	4822 051 10102	1k 2% 0,25W
3598	4822 117 10833	10k 1% 0,1W
3599	4822 117 10833	10k 1% 0,1W

## COILS

5501	4822 157 70601	100μH (920927085A)
5504	4822 242 10756	DSS306-92Y5S221M100
5505	4822 242 10756	DSS306-92Y5S221M100
5507	4822 242 10756	DSS306-92Y5S221M100
5508	4822 242 10756	DSS306-92Y5S221M100
5509	4822 242 10756	DSS306-92Y5S221M100
5510	4822 242 10756	DSS306-92Y5S221M100
5511	4822 242 10756	DSS306-92Y5S221M100
5512	4822 242 10756	DSS306-92Y5S221M100
5513	4822 242 10756	DSS306-92Y5S221M100

**DIODES**

6501	4822 130 11087	BZX284-C15
6502	4822 130 11087	BZX284-C15
6503	4822 130 11087	BZX284-C15
6504	4822 130 11087	BZX284-C15
6505	4822 130 11087	BZX284-C15
6506	4822 130 11087	BZX284-C15

**TRANSISTORS & IC's**

7501	4822 209 32071	MC33079D
7503	4822 209 33403	TDA1305T/N2
7520	4822 130 42616	BC818-40
7521	4822 130 42616	BC818-40
7522	4822 130 42616	BC818-40
7523	4822 130 42616	BC818-40
7525	5322 130 41983	BC858B
7526	5322 130 41982	BC848B
7527	5322 130 41982	BC848B
7528	5322 130 41983	BC858B
7529	5322 130 41982	BC848B
7530	5322 130 41982	BC848B
7531	5322 130 41983	BC858B
7532	5322 130 41982	BC848B
7533	5322 130 41982	BC848B
7534	5322 130 41983	BC858B
7535	5322 130 41982	BC848B
7536	5322 130 41982	BC848B
7537	5322 130 41983	BC858B
7538	5322 130 41982	BC848B
7539	5322 130 41982	BC848B